

WARRANTY REGISTRATION CARD

Name _____ Address _____ Zip _____
Product purchased RFC 8-AP Serial No. 840 01020
KANTRONICS Date purchased _____

1. Have you ever purchased a Kantronics product before? ☐ Yes ☐ No

If yes, what product(s) did you purchase? _____

2. What is your age? ☐ under 20 ☐ 20 to 40 ☐ 40 to 60 ☐ over 60

3. How long have you had your license? _____ What is your license class?

☐ Novice ☐ Technician ☐ General ☐ Advanced ☐ Extra

4. How did our product come to your attention?

☐ Through a friend ☐ At a dealer ☐ Ad ☐ At a Hamfest ☐ In a catalog

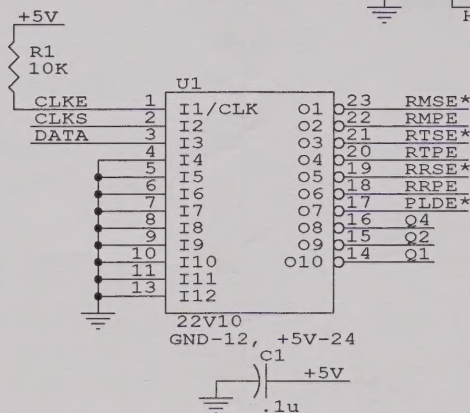
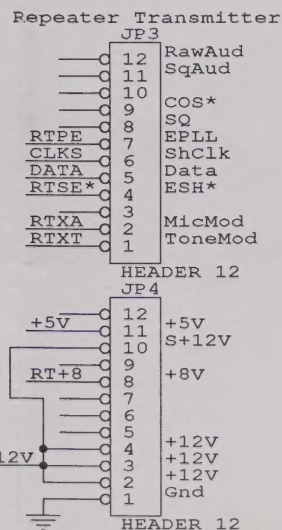
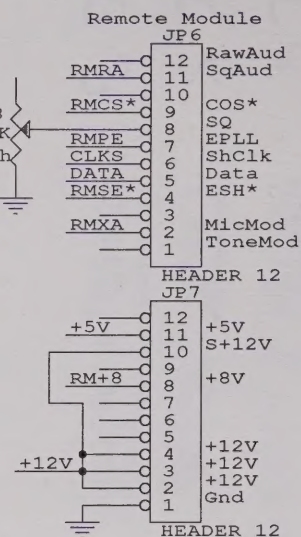
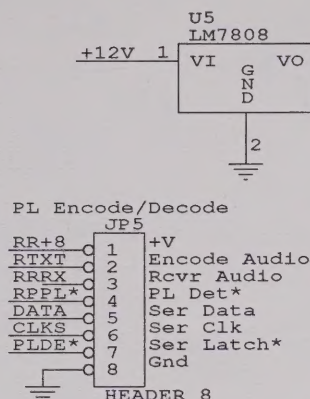
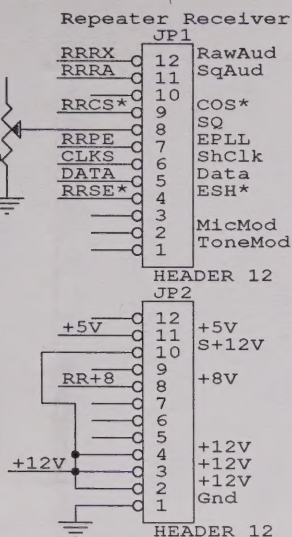
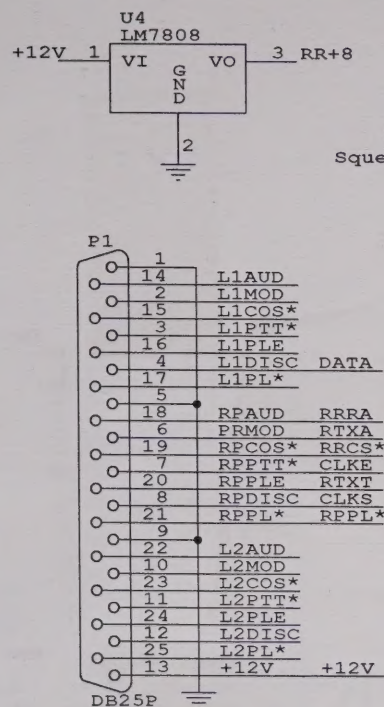
5. If through a magazine, what magazine(s)? ☐ CQ ☐ QST ☐ 73 ☐ Worldradio ☐ Ham Radio

6. Where did you purchase this product? _____

Comments:

Please send a copy of your sales slip with this card to protect this warranty.





- Notes: (1) Module connectors as seen from bottom of module PCB, in pin order
(2) Add jumpers on controller PCB: U14/4-P1/8 and U14/5-P1/4
(3) Supply +12V through transmitters
(4) Change controller R9 to 4.7K

The Buaas Corporation

Size	Document Number	REV
A	Repeater/Remote using TM-741 Modules	00
Date:	August 16, 1993	Sheet 1 of 1

PC4 RPT / LINK + REM

PC 5 LINK / REM

PC 3 RPTR FUNCTION

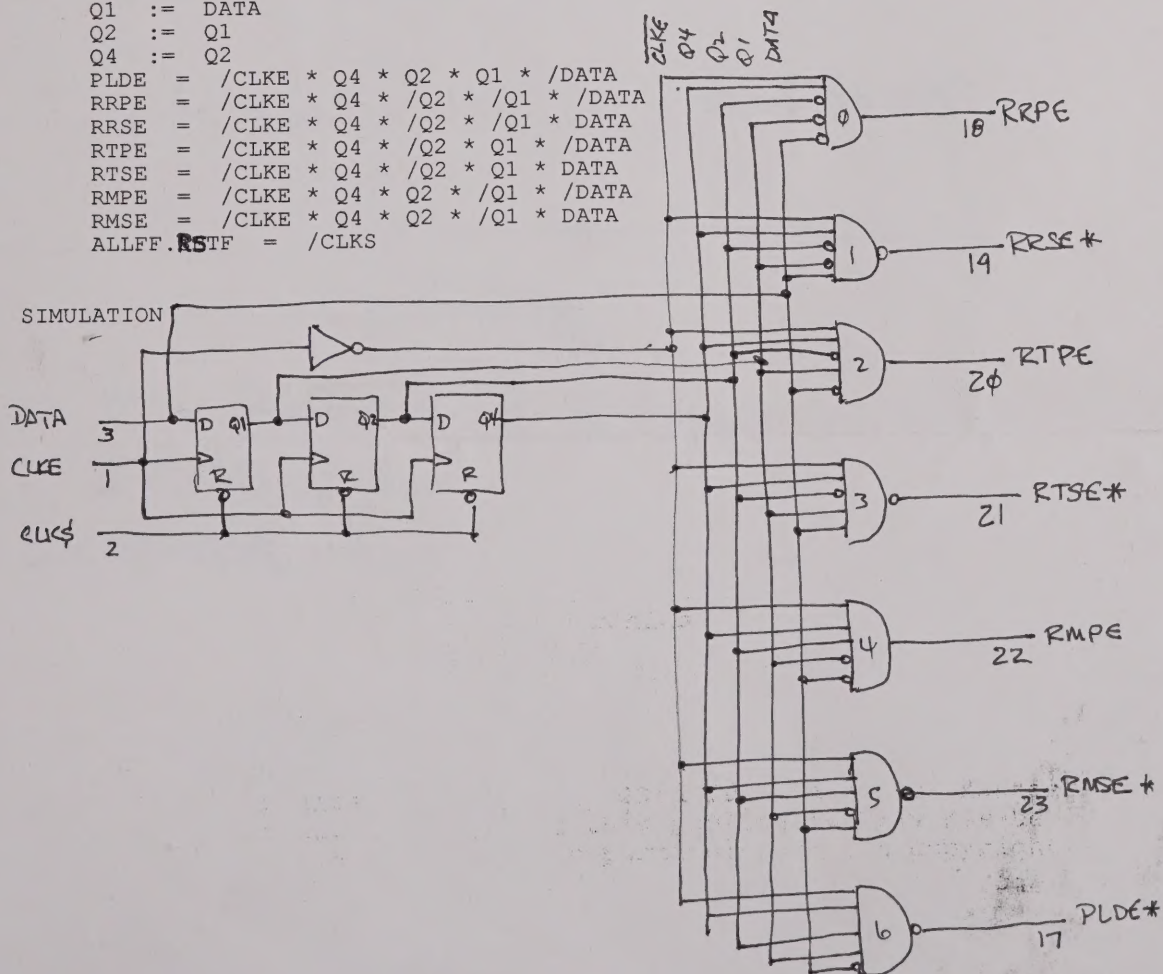
TITLE Contro three TM-741 modules
PATTERN
REVISION 01
AUTHOR Robert Buaas
COMPANY The Buaas Corporation
DATE August 14, 1993

CHIP CTL741 PAL22V10

PIN 1 CLKE
PIN 2 CLKS
PIN 3 DATA
PIN 12 GND
PIN 14 Q1
PIN 15 Q2
PIN 16 Q4
PIN 17 PLDE LOW
PIN 18 RRPE
PIN 19 RRSE LOW
PIN 20 RTPE
PIN 21 RTSE LOW
PIN 22 RMPE
PIN 23 RMSE LOW
PIN 24 VCC
NODE 1 ALLFF

EQUATIONS

Q1 := DATA
Q2 := Q1
Q4 := Q2
PLDE = /CLKE * Q4 * Q2 * Q1 * /DATA
RRPE = /CLKE * Q4 * /Q2 * /Q1 * /DATA
RRSE = /CLKE * Q4 * /Q2 * /Q1 * DATA
RTPE = /CLKE * Q4 * /Q2 * Q1 * /DATA
RTSE = /CLKE * Q4 * /Q2 * Q1 * DATA
RMPE = /CLKE * Q4 * Q2 * /Q1 * /DATA
RMSE = /CLKE * Q4 * Q2 * /Q1 * DATA
ALLFF.RSTF = /CLKS



Motorola SHW158 @ 444G
 drive current voltage output eff.
 4.8w 4.1 12.3 20w 5043 39.7%

0.5w 3.1 12.6 17w 43.5%

@ 420.575

4w 4.45 12.45 16.3 30.1%

+25.575 4w 4.4 12.3 17.5 32.3%
 $-1 = 10 \log \frac{P_o}{P_i}$

$$17 \cdot 10^{-1} = 13.5 \text{ v}$$

34.5% eff w/filter circ loss

T44 R5A

44w 144 30.5% eff

Controller

0519 260ms

27028 215ms

27028+85025 145ms

T34RTA

30w	11.5a @ 13.8
25w	10a @ 13.8
20w	9a @ 13.8
15w	7.9a @ 13.8
stbg	322ma
2w	1.07a

T44RTA

stbg	258ma
37.4	11.9a
28w	10a
23.5	9a
16.8	7.9a

Power requirements

	std by	xmit
control	.75a	
UHF rxptr	.5a	13a
link	.5a	13a
remote	.5	2.5

rx $2a \times 24hr = 48ah -$
 ~~$26a \times 1hr = 26ah$~~

tx $39a \times 3hr = 117$

10.8

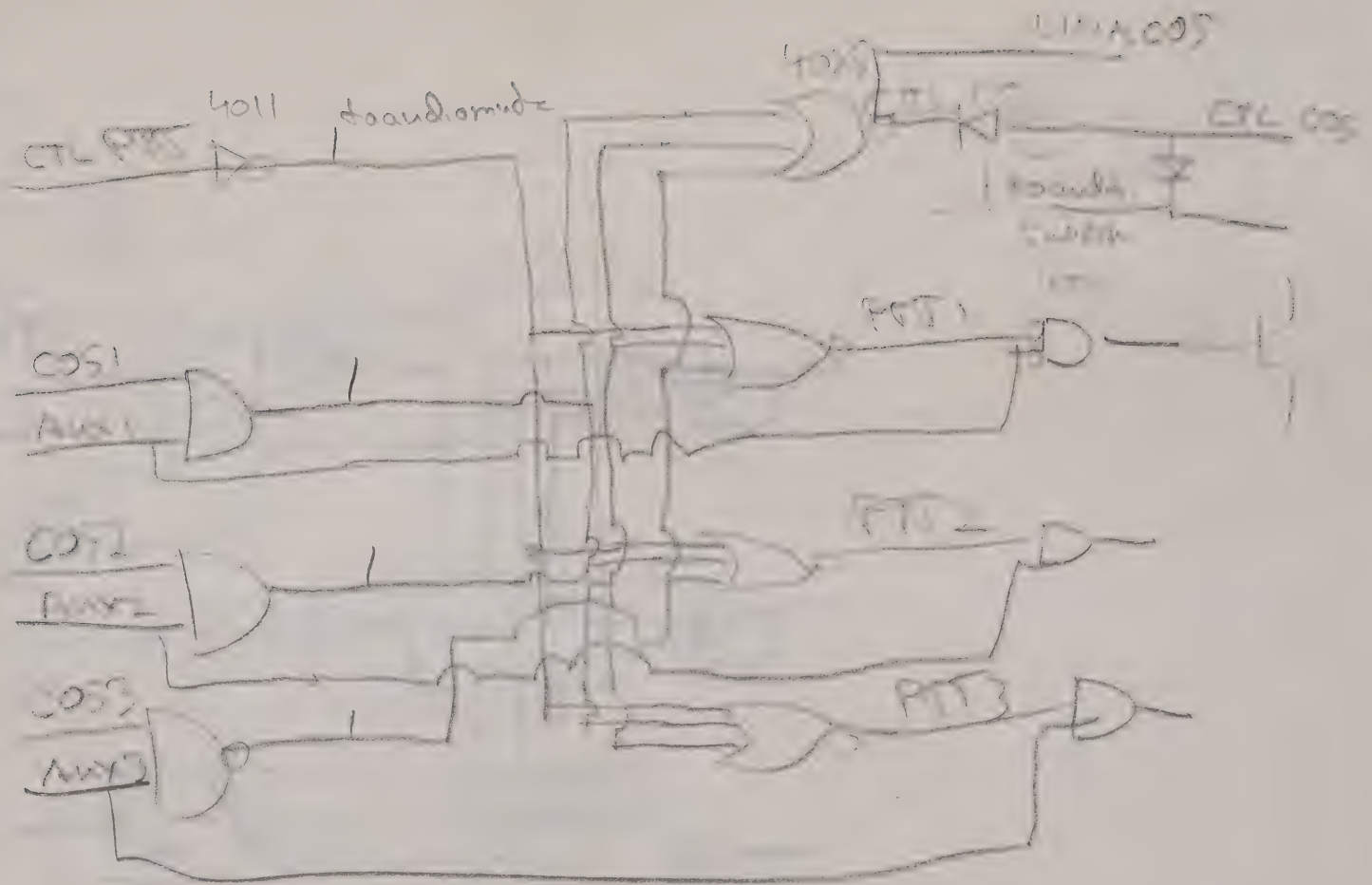
$= 2 \times 2 \quad 12w -$
 $- 4 \times 8 -$

~~$7a \times 24hr$~~ $168ah$

$7a \times 10$ $70ah$
 $\underline{1.3}$

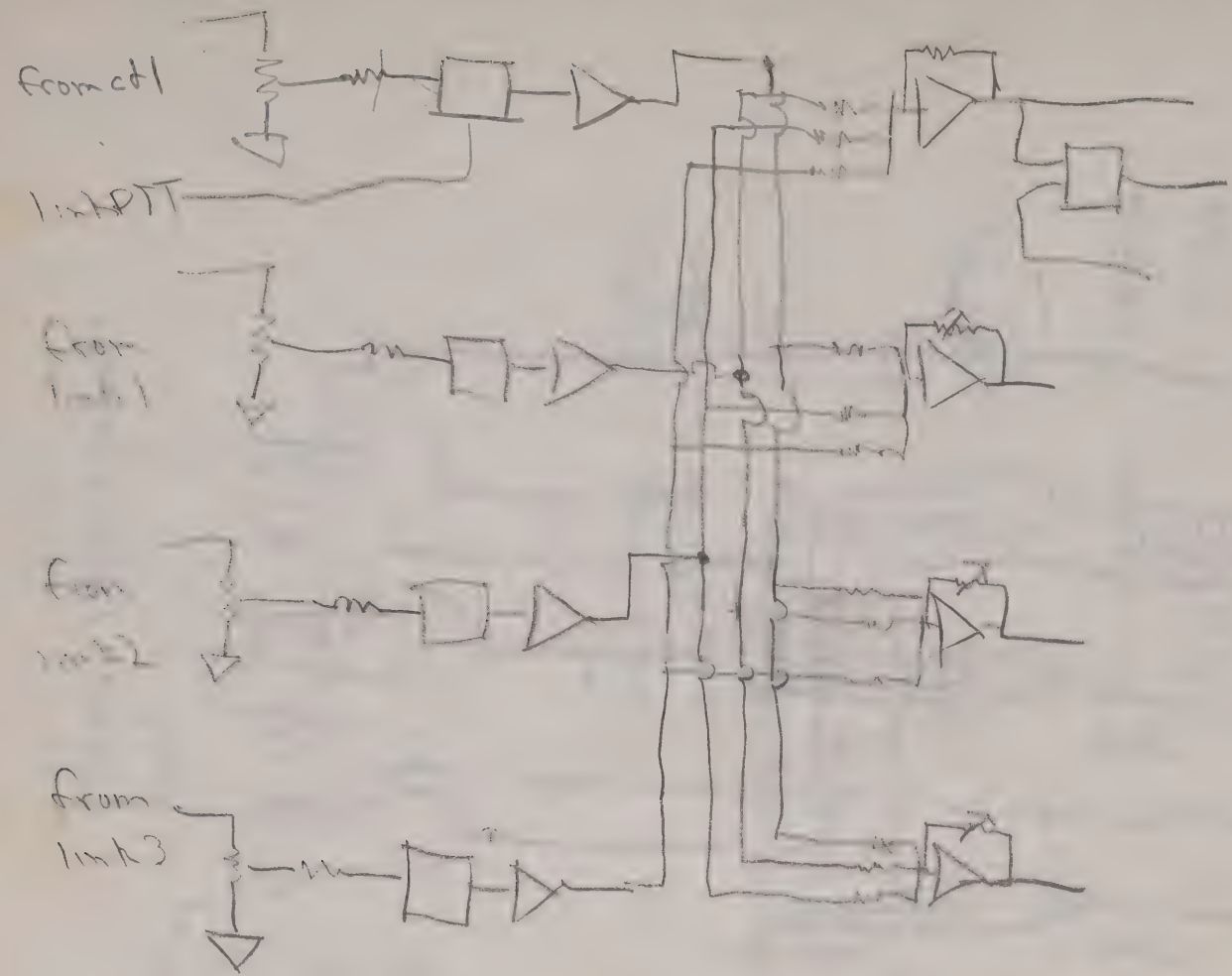
$3 \times 3 = 9w$ $\underline{210.}$
 $\underline{700}$

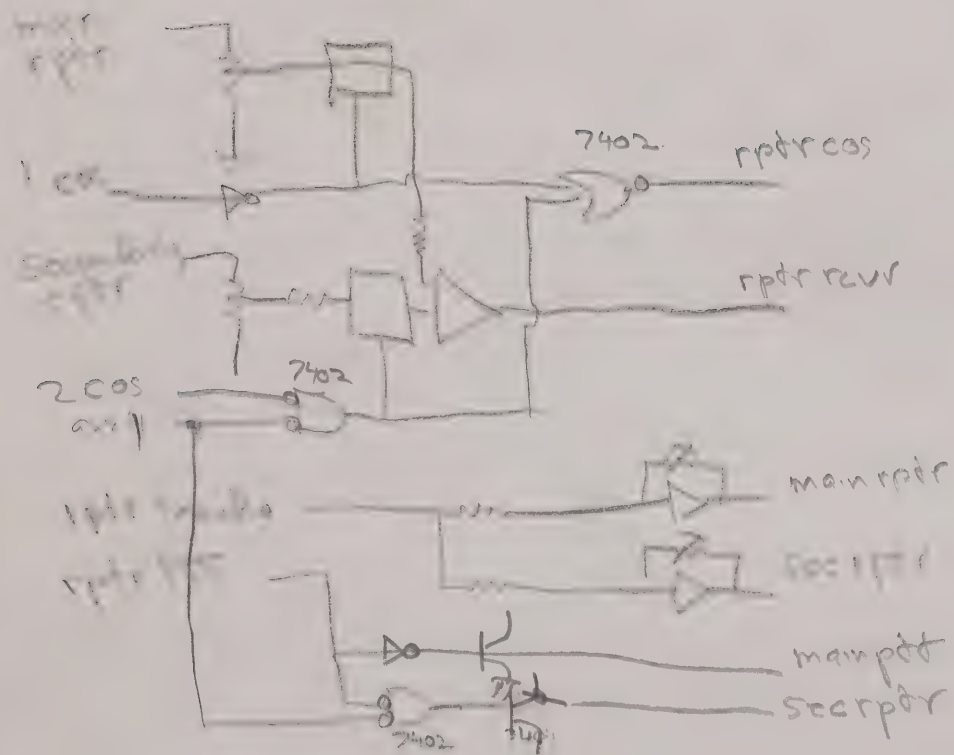
~~$913ah$~~

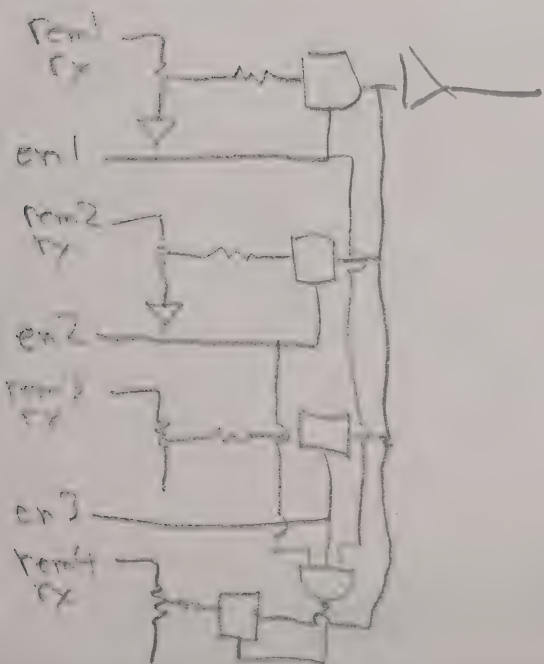
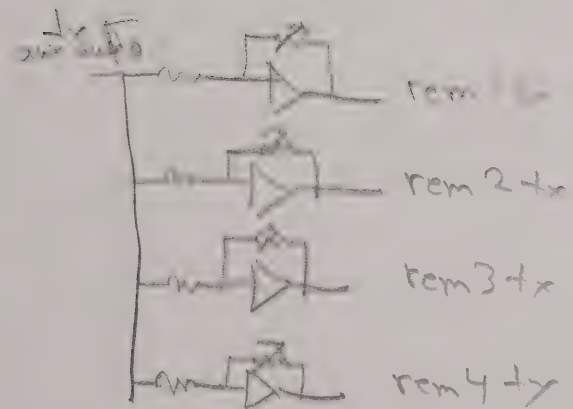
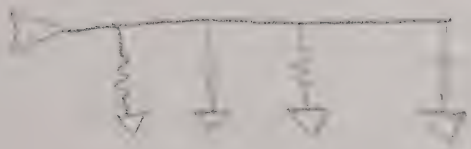


3 DE

900 - 538 - 5000 for 408 - 585 - 0250







Item	Quantity	Reference	Part
1	16	C1,C2,C5,C6,C7,C11,C12, C13,C14,C25,C26,C27,C28, C29,C30,C31	.1
2	3	C8,C9,C10	10UF
3	10	C15,C16,C17,C18,C19,C20, C21,C22,C23,C24	.01
4	6	D1,D2,D3,D4,D5,D6	D1N4148
5	3	Q1,Q2,Q3	Q2N2222A
6	18	R1,R7,R9,R22,R23,R24,R25, R26,R28,R29,R31,R32,R40, R58,R60,R62,R66,R69	56K
7	7	R2,R10,R59,R61,R63,R64, R65	200K
8	8	R4,R34,R35,R36,R37,R38, R39,R68	560K
9	14	R8,R11,R27,R30,R33,R42, R43,R46,R48,R49,R51,R52, R67,R70	100K
10	2	R12,R21	5.6K
11	1	R20	47
12	7	R41,R44,R45,R47,R50,R53, R54	10K
13	3	R55,R56,R57	1K
14	2	U1,U7	4053
15	2	U2,U8	LM3900N
16	1	U3	4011
17	2	U4,U5	4025
18	1	U6	4001

0.0
0.1
0.2
0.3
0.4
0.5
0.6
0.7
0.8
0.9
1.0

-1-

A 2.1

7 ✓ A7 7970 125
5 3 17

EN 2 400
600

A 21 - 1
↓
→

Printed
AOL - 500
107 5 500

AG142 (W)

A71

1175

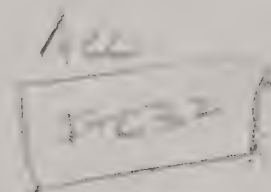
1175

8/1/75

124 0000

Tx + Rx

1175



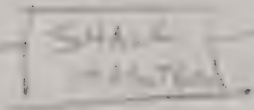
(LOCK)
(TIMERS)
(ON-OFF)
(SERIAL)

PTT (PPTX) (FET)

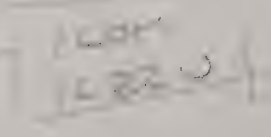
PTT (LINK) (FET)

COS (PPTX) (ACTIVE LO)

COS (LINK) (ACTIVE HI)

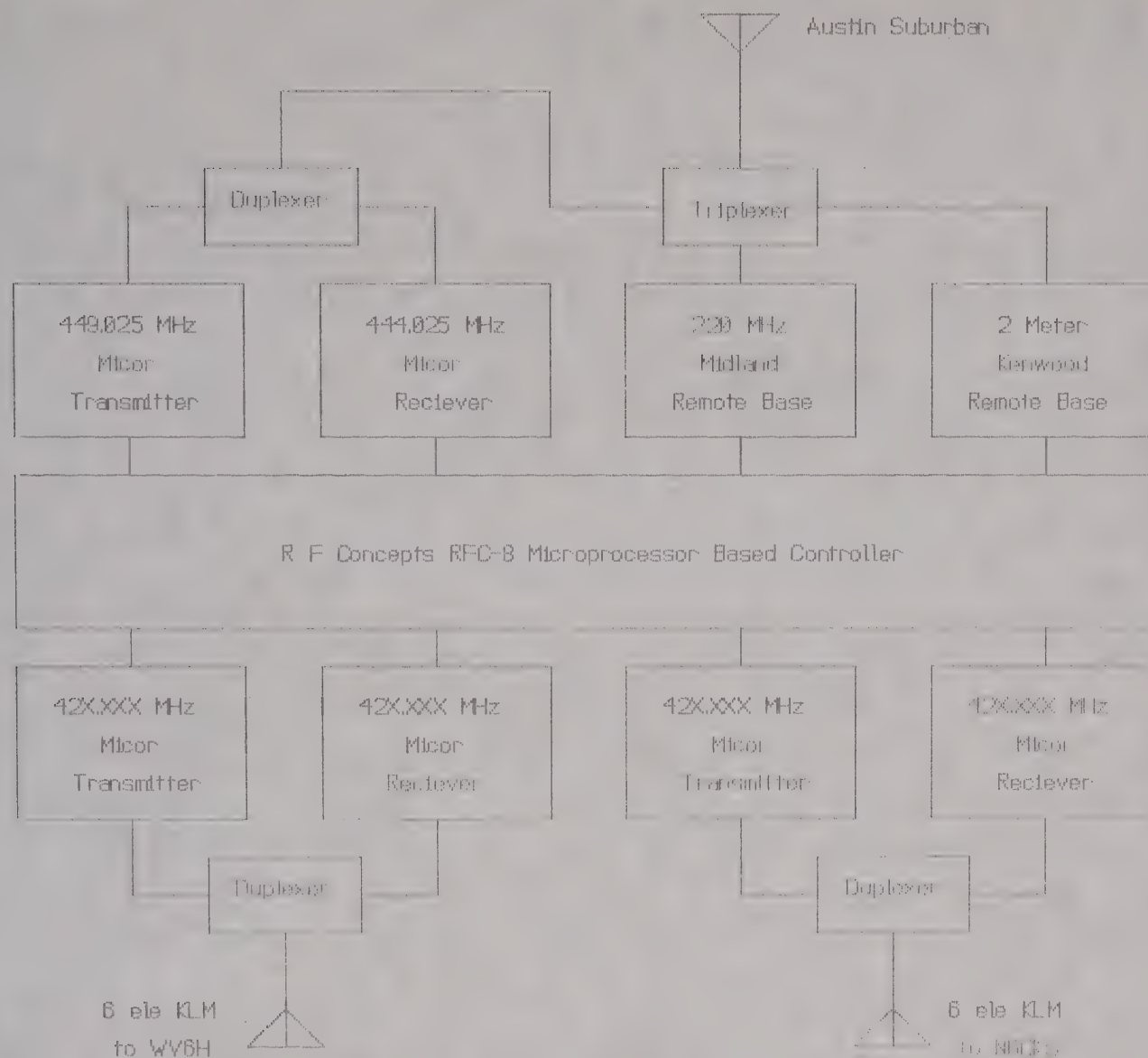


SERIAL
BIO FIBER
CONTROL

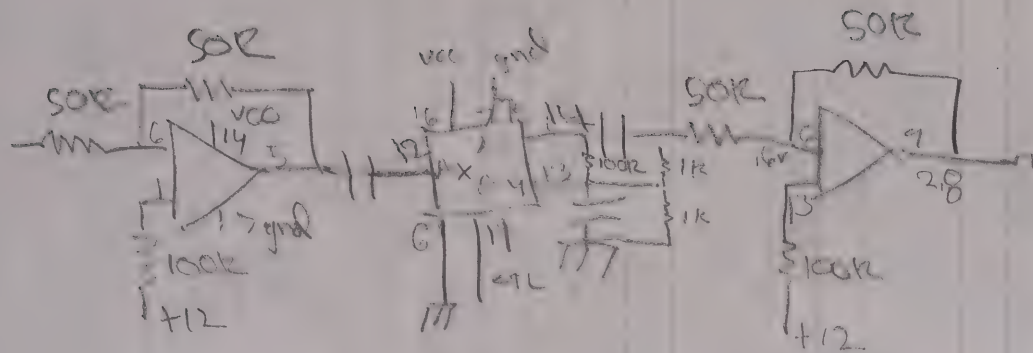




Hondrix Real System Block Diagram



RF parts - SAM macos



T1 - $5V \pm 12V$

4" x 4" 4pin molex
slide switch xfmr toroid
bridge

National LM1 series

INTRODUCTION	1-1
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WARNING: This product contains static sensitive components.
 Take proper precautions to prevent static buildup
 while handling.

The RF Concepts RFC 8-RC Repeater Controller represents a different approach to repeater control. The RFC 8-RC was designed with emphasis placed on being a very flexible and powerful workhorse instead of providing fancy 'Bells and Whistles'. The result is a control system that can be expanded to handle all the requirements of large, multiple-site, interconnected systems as well as the simple repeater. The operation of the RFC 8-RC is straight forward and totally transparent to the everyday user.

The RFC 8-RC Repeater Controller provides all functions required for standard repeater operation. In addition, facilities are provided for a control receiver, link system, multiple remote bases, 8 auxiliary on/off outputs, CTCSS decoder input, and an alarm input to signal conditions such as power failure or open door.

All command codes are remotely programmable as are the various timers, tone pitches, and the ID message. All data is stored in non-volatile EEPROM so battery backup is not required to maintain operating parameters in case of power failure. All commands to the controller are verified with a CW message. The controller may be used as a basic repeater control system or may be the heart of a super system with a multi-channel link, multiple synthesized remote bases and autopatch with the addition of various optional accessories.

To allow for different applications the RFC 8-RC provides two different system operating modes. Both modes include ten user programmable operating modes and two different configurations for the link channel as well as simplex or duplex link operation. The link/remote base cross-connect may be switched on and off or the link/remote base may be setup to operate to control a remote autopatch.

SYSTEM MODE 1. The auxiliary output port is used for direct on/off control of up to eight external functions. In this mode there are no facilities for an autopatch or changing link or remote base frequencies.

SYSTEM MODE 2. The RFC 8-RC provides support for the RFC 8-AP Autopatch, RFC 8-RP Remote Autopatch Interface, up to eight RFC 8-RB Remote Base Interfaces, RFC 8-LI Link Interface Board, RFC 8-AX Auxiliary Expansion, and the RFC 8-PK Packet Interface which allows control via packet with installation of an external TNC and transceiver. When using SYSTEM MODE 2 the RFC 8-RC provides ten memory channels to store information for a synthesized remote base. Each memory channel contains the remote base #, frequency, offset and sub-audible tone, if any.

The repeater, link, and remote base receiver inputs are arranged in a priority scheme that allows each input to be repeated out the other two. If a signal arrives on an input with a higher priority than the one currently active, the signal with the higher priority takes precedence. This allows signals from the remote base to be relayed to distant users on the link channel and distant users to communicate with others on either the repeater or remote base via the link channel. The highest priority is given to the repeater receiver and the lowest to the remote base receiver.

Listed below are options that will be available:

The RFC 8-AP will provide a complete autopatch including the ability to control the RFC 8-RC via the telephone line as well as reverse autopatch capability. The RFC 8-AP regenerates all DTMF tones and has an autodial memory that will hold 100 different telephone numbers as well as a last number redial feature. An activity timer which may be switched on or off and a method to restrict calls to the local calling area are also provided. The RFC 8-AP also contains the circuitry to decode the 8 Aux Outputs and the Channel Select Outputs for the link radio.

The RFC 8-RP provides the interface circuitry to allow transparent and automated access to an autopatch not located at the repeater site.

The RFC 8-RB Remote Base Interface contains circuitry to interface the RFC 8-RC to many different types of synthesized transceivers. It also contains a remotely programmable CTCSS encoder. The RFC 8-RB may be used for control of equipment connected to either the link or remote base port of the RFC 8-RC.

The RFC 8-AX Auxiliary Expansion Interface increases the number of auxiliary on/off outputs from eight to forty. It allows each group of eight outputs to be configured with a single command and two eight bit ports may be configured to drive external CTCSS encoder/decoders.

The RFC 8-PK packet interface provides a communications link between the RFC 8-RC controller and an external TNC. This will allow control of the RFC 8-RC via a packet radio link.

The RFC 8-SI Serial Interface can be used to decode either the Link Channels or the Aux Outputs.

SPECIFICATIONS

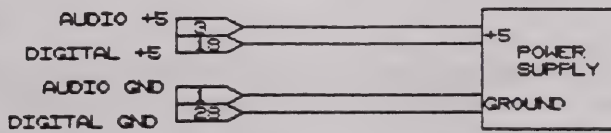
Audio Input Level	-10 dbm at 3 KHz Deviation (.25v RMS)
Input Impedance	Greater than 50K ohms
Audio Output Level	-10 dbm for 3 KHz Deviation (.25v RMS)
COS Inputs	CMOS Buffered - Active Low
Alarm Input	TTL - Active Low
CTCSS Decoder Input	CMOS Buffered - Active High
PTT Outputs	Open-collector Transistor - Active Low will sink 30 VDC at 100 mA
Aux/Expansion Port	Eight bits - Open collector/Active Low
Hang Delay Timers	Programmable from .05 to 4.0 Seconds
Time-out Timers	Programmable from .5 to 3.0 Minutes
Tone Frequencies	Programmable from 400 to 3000 Hz
CW Speed	Programmable from 10 to 30 WPM
User Programmed Operating Modes	Ten
Links	One (Up to eight channels with RFC 8-AP or RFC 8-SI)
Remote Bases	One (Up to eight with RFC 8-RB)
Microprocessor	8085A (1.6 MHz)
Memory	16384 Bytes ROM 8192 Bytes NOVRAM 256 Bytes RAM
Power Requirements	5 Volts D.C. at less than 300 mA
Size	4.5 X 6.5 Inches
Connector	36/72 Pin X .100 Spacing

REPEATER INSTALLATION

In addition to power, four other connections are required for basic repeater operation. Two signals from the repeater receiver and two from the repeater transmitter.

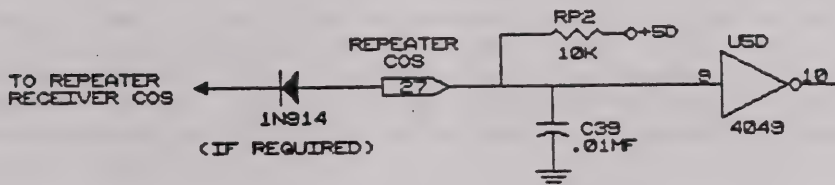
POWER SUPPLY

The RFC 8-RC requires a power supply of 5 volts DC (+/- .25V) at 300 mA. This may be obtained from the repeater or a separate supply. The RFC 8-RC has several terminals for power and ground. These should be connected together ONLY at the power supply to prevent digital noise from appearing on the audio line.



COS (Carrier-Operated-Switch)

This is a signal from the repeater receiver that indicates there is a signal present. This signal is present in most receivers designed for repeater service. If your receiver does not have a COS output you will have to provide one. The place to look is at the noise detector part of the squelch circuit or at the audio switch. The RFC 8-RC requires a COS signal that goes to ground when the receiver is active. This may be an open collector type output, preferred, or a logic type output. If this output has any voltage present during receiver inactivity a diode will be required for isolation as shown in the example below.



Thermodynamics

The first law of thermodynamics states that energy is conserved. It can be expressed as:

$$\Delta U = Q - W$$

where ΔU is the change in internal energy, Q is the heat added to the system, and W is the work done by the system. This law is a statement of the conservation of energy.

The second law of thermodynamics states that the entropy of an isolated system always increases over time. It can be expressed as:

$$\Delta S \geq 0$$

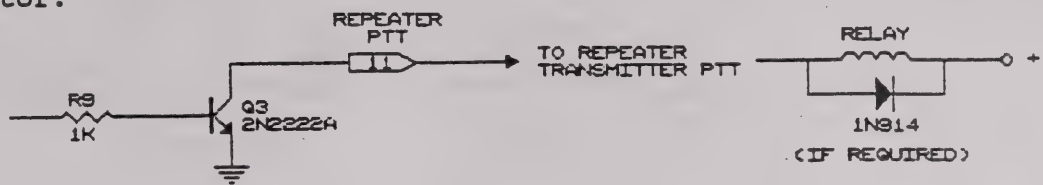
where ΔS is the change in entropy. This law is a statement of the irreversibility of natural processes. It implies that the total entropy of the universe is always increasing.

The third law of thermodynamics states that the entropy of a perfect crystal at absolute zero is zero. It can be expressed as:

$$S = 0 \text{ at } T = 0$$

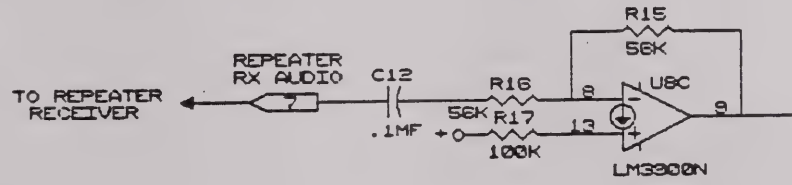
PTT (Push-to-Talk)

This signal is an output from the RFC 8-RC to turn on the repeater transmitter. The RFC 8-RC controller provides a solid-state closure to ground. This output can sink up to 100 mA when on and withstand 30 volts DC when off. If your transmitter has different requirements than those above the PTT output can be used to drive a relay to switch the transmitter on and off. If your transmitter is switched by a relay be sure to install a diode across the relay coil to prevent damage to the driver transistor.



RECEIVER AUDIO

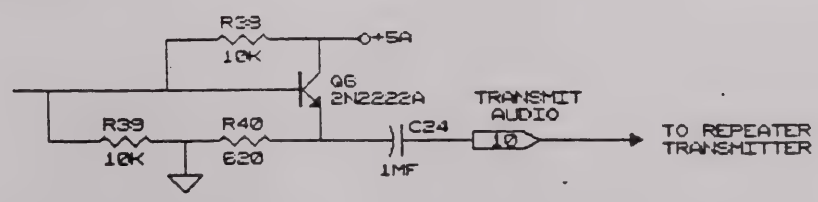
Audio needs to be supplied by the repeater receiver to the RFC 8-RC controller. This audio should be de-emphasized and after the squelch gate. The level required by the controller is -10 dbm (.25v RMS) with a 3 KHz deviated signal into the receiver. The input circuitry is capacitive coupled with an impedance greater than 50K ohms so there should not be any problem with loading.



TRANSMITTER AUDIO

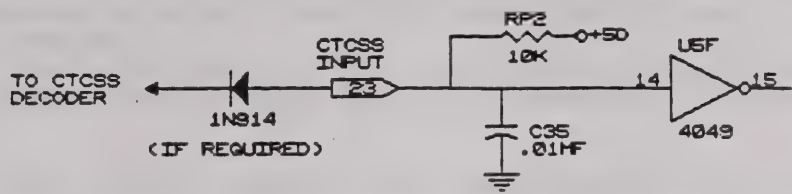
The RFC 8-RC supplies all audio to the repeater, link. and remote base transmitters. The output level is -10 dbm (.25v RMS) to produce 3 KHz of deviation. The output of the controller board is low impedance and capacitive coupled. If your transmitter requires more drive you will have to install an amplifier of some kind. You may use the microphone input but it may be necessary to install an attenuator to prevent overdriving the speech amplifier. After the repeater installation is complete, adjust R15 on the RFC 8-RC board for the desired tone level (ID's. etc.).

The TX AUDIO OUTPUT is muted when the Command Tones are sent. The AUX AUDIO OUTPUT is not muted and can be used to pass DTMF tones through link interconnects or for control of a remote autopatch. However, it may need an external amplifier.



CTCSS DECODER

The RFC 8-RC provides an input for a CTCSS Decoder.
If this input is used, it needs to be held low (ground) when the proper TCSS tone is not present. When the tone is present, the decoder output needs to switch to either a high impedance condition (open-collector output) or to +5 volts (TTL/CMOS logic output).



OPERATION

COMMANDING THE CONTROLLER

Commands for the RFC 8-RC are divided into three groups. These groups are arranged to provide different levels of security for your control codes. The first group is the Setup Command Group. These are the commands for programming the timers, command prefixes, ID message, etc..

The second group is the Control Operator Command Group. These are the commands to select operating modes and to enable or disable operating parameters.

The third group is the User Command Group. These include functioning the Link, Remote Base, Auxiliary Functions, Autopatch, etc..

The Control Operator and User Commands all have the same format.

PREFIX CODE followed by a COMMAND CODE

XXXX - XXXXX

1 to 4 digits - 1 to 5 digits

Commands may be entered through the repeater or control receiver. When the control receiver COS is active, control will not be allowed through the repeater receiver. Commands entered through the repeater receiver will be acknowledged in CW. Commands entered through the control receiver port will not be acknowledged unless enabled by the Auxiliary Control Command. Activation of the control receiver will erase any commands being entered on the repeater receiver. The RFC 8-RC normally evaluates tone entries upon squelch closure. However, you may force evaluation by ending your command string with the "#". This will cause immediate command evaluation and will not generate a CW response unless the Auxiliary Control function is enabled.

There are several other conditions concerning command entry. Once you begin entering a command you must complete it within 15 seconds. The only exception is when programming the ID message. When programming the Command Prefixes you must begin entering the new prefix within 10 seconds after entering the "Set Prefix" commands or you will have to start over.

SYSTEM DEFAULTS

The RFC 8-RC comes with a series of default (preset) Prefixes, Functions, and Tones. These defaults are listed on page B-1. Any or all of these defaults may be changed using the Setup procedure.

TIME-OUT TIMER

This timer is used to turn the system off in the event a steady signal remains on any of the system inputs excluding the control receiver. The time-out timer may be enabled or disabled separately for the repeater, link, or remote base inputs. If the courtesy tone is enabled, the time-out timer will reset on the tone otherwise it is reset when the input signal disappears or the controller switches to a different receiver input. When a time-out is ready to occur a warning tone will be transmitted on the active transmitters to warn listeners of the impending time-out. If a time-out occurs, the time-out timer will reset when the input signal disappears for 1/2 second. The duration of this timer is programmable from 30 sec. to 3 min. in 30 second increments.

ID'er

The RFC 8-RC is set to ID every 6 minutes. The first ID is sent at the end of the first transmission. If there is continued activity the ID will be sent at the end of the first transmission after the 6 minute interval has expired. If this transmission lasts beyond 6 minutes, to 9 minutes, the repeater will "Time Out" and identify.

If there is no activity the ID'er resets and an ID will not occur until the end of the next transmission.

COURTESY TONE

When the courtesy tone system is enabled, a beep will be sent 600 ms after the squelch closes. A different tone pitch may be selected for the repeater, link, and remote base inputs to signal users which receiver the signal came through. The time-out timer is reset on the beep. If the courtesy tone system is disabled the time-out timer will reset immediately on squelch closure or if the controller switches to a different receiver input. There will be no courtesy tone if the hang time for that particular receiver is set to less than 1.5 second.

PRIVACY TONE

When this mode is enabled a pulsing tone will be generated while commands are being entered through the repeater receiver. This provides for security of your control codes and a pleasant tone that will not bother listeners.

KERCHUNK AND NOISE FILTERING

The kerchunk filter will immediately drop the transmitter upon squelch closure on any transmissions less than 500 ms in length. Also provided is a delayed PTT which filters against noise pulses on the COS inputs. The PTT lines will not be activated until a signal has been present for 60 ms.

T-P (Touch-Pad) ACCESS

When the T-P ACCESS mode is activated the user must send a turn-on code from a Touch-Tone(*) pad to activate the Repeater. The Repeater will then operate in a normal manner. When activity stops, the repeater will reset to T-P ACCESS. The time it takes to reset is adjustable.

* "Touch-Tone" is a registered trademark of A.T. and T..

ACCESS (Carrier or CTCSS tone)

The RFC 8-RC has four access modes. One is "carrier access". The other three require an input from the CTCSS tone decoder in the receiver.

SETUP COMMANDS

Before any of the following SET UP COMMANDS can be used, you must enter your unique nine digit unlock code. The RFC 8-RC will respond in CW with "OK" and remain unlocked for 60 seconds. If no Setup Commands are entered for a period exceeding 60 seconds the RFC 8-RC will relock itself. After entry of any of the following commands the Setup Timer will be reset for another 60 seconds. See page A-1 for a summary of the commands.

UNLOCK CODE

Note: This code is unique to your controller and is not used on any other controller.

ID PROGRAMMING: (Default CALL/R)

To program your ID message enter '*8090', wait for the acknowledgment "ID OK" then enter the two-digit codes for the characters in the message. DO NOT enter the '/R'. This will be added automatically. If you entered a valid sequence the RFC 8-RC will read the new ID message back to you in CW.

CHARACTER CODES:	0 = 00	9 = 09	I = 18	R = 27
	1 = 01	A = 10	J = 19	S = 28
	2 = 02	B = 11	K = 20	T = 29
	3 = 03	C = 12	L = 21	U = 30
	4 = 04	D = 13	M = 22	V = 31
	5 = 05	E = 14	N = 23	W = 32
	6 = 06	F = 15	O = 24	X = 33
	7 = 07	G = 16	P = 25	Y = 34
	8 = 08	H = 17	Q = 26	Z = 35

SETTING TONES:

TONE CHART:	0 = 400 Hz	5 = 1225 Hz
	1 = 500 Hz	6 = 1530 Hz
	2 = 625 Hz	7 = 1910 Hz
	3 = 780 Hz	8 = 2375 Hz
	4 = 975 Hz	9 = 2980 Hz

ID'er TONE (Default 1225 Hz)

To set the pitch of the ID'er enter '*4560x' where 'x' = 0-9 for the desired tone from the Tone Chart. The RFC 8-RC will respond in CW with "IDT OK".

REPEATER COURTESY TONE (Default 625 Hz)

To set the pitch of the repeater courtesy tone enter '*4561x' where 'x' = 0-9 for the desired tone from the Tone Chart. The RFC 8-RC will respond in CW with "CT1 OK".

The following table shows the results of the experiments conducted during the year 1914-1915. The experiments were conducted in the laboratory of the Department of Agriculture, and the results are given in the following table.

The results of the experiments show that the following factors are of importance in the production of the crop: (1) the amount of water, (2) the amount of fertilizer, (3) the amount of labor, and (4) the amount of seed.

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Amount of water			
1	2	3	4
5	6	7	8
9	10	11	12
13	14	15	16
17	18	19	20
21	22	23	24
25	26	27	28
29	30	31	32
33	34	35	36
37	38	39	40
41	42	43	44
45	46	47	48
49	50	51	52
53	54	55	56
57	58	59	60
61	62	63	64
65	66	67	68
69	70	71	72
73	74	75	76
77	78	79	80
81	82	83	84
85	86	87	88
89	90	91	92
93	94	95	96
97	98	99	100

The results of the experiments show that the following factors are of importance in the production of the crop: (1) the amount of water, (2) the amount of fertilizer, (3) the amount of labor, and (4) the amount of seed.

Amount of fertilizer			
1	2	3	4
5	6	7	8
9	10	11	12
13	14	15	16
17	18	19	20
21	22	23	24
25	26	27	28
29	30	31	32
33	34	35	36
37	38	39	40
41	42	43	44
45	46	47	48
49	50	51	52
53	54	55	56
57	58	59	60
61	62	63	64
65	66	67	68
69	70	71	72
73	74	75	76
77	78	79	80
81	82	83	84
85	86	87	88
89	90	91	92
93	94	95	96
97	98	99	100

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LINK COURTESY TONE (Default 780 Hz)

To set the pitch of the link courtesy tone enter '*4562x' where 'x' = 0-9 for the desired tone from the Tone Chart. The RFC 8-RC will respond in CW with "CT2 OK".

REMOTE BASE COURTESY TONE (Default 975 Hz)

To set the pitch of the remote base courtesy tone enter '*4563x' where 'x' = 0-9 for the desired tone from the Tone Chart. The RFC 8-RC will respond in CW with "CT3 OK".

COMMAND ACKNOWLEDGMENT TONE (Default 1910 Hz)

To set the pitch of the acknowledgment tone enter '*4564x' where 'x' = 0-9 for the desired tone frequency from the Tone Chart. The RFC 8-RC will respond in CW with "ACK OK".

PRIVACY TONE (Default 400 Hz)

To set the pitch of the privacy tone enter '*4565x' where 'x' = 0-9 for the desired tone from the Tone Chart. The RFC 8-RC will respond in CW with "PT OK".

SETTING HANG TIMES:

HANG TIME CHART:	0 = .05 Sec	5 = 2.0 Sec
	1 = .25 Sec	6 = 2.5 Sec
	2 = .50 Sec	7 = 3.0 Sec
	3 = 1.00 Sec	8 = 3.5 Sec
	4 = 1.50 Sec	9 = 4.0 Sec

(NOTE: Hang times shorter than 1.5 second will not generate a courtesy tone.)

REPEATER HANG TIME (Default 1.5 sec.)

To set the repeater hang time enter '*7410x' where 'x' = 0-9 for the desired delay time from the Hang Time Chart. The RFC 8-RC will respond in CW with "HT OK".

LINK HANG TIME (Default 1.5 sec.)

To set the link hang time enter '*7411x' where 'x' = 0-9 for the desired delay time from the Hang Time Chart. The RFC 8-RC will respond in CW with "LT OK".

REMOTE BASE HANG TIME (Default 1.5 sec.)

To set the remote base hang time enter '*7412x' where 'x' = 0-9 for the desired delay time from the Hang Time Chart. The RFC 8-RC will respond in CW with "RT OK".

SETTING TIME-OUT TIMERS:

TIME-OUT CHART:	0 = .5 Min	3 = 2.0 Min
	1 = 1.0 Min	4 = 2.5 Min
	2 = 1.5 Min	5 = 3.0 Min

TIME-OUT TIMER (Default 3 min.)

This command is used to set the length of the time-out timer. To set this timer enter '*7413x' where 'x' = 0-5 for the desired time from the Time-out Chart. The RFC 8-RC will respond in CW with "TO OK".

T-P (Touch Pad) ACCESS TIME-OUT TIMER (Default 1 min.)

This command is used to set the length of time the repeater will remain enabled without activity when the T-P Access Mode is enabled. To set this timer enter '*7414x' where 'x' = 0-5 for the desired time from the Time-out Chart. The RFC 8-RC will respond in CW with "ATO OK".

AUTOPATCH ACTIVITY TIMER (Default 1 min.)

To set the timer enter '*7415x' where 'x' = 0-5 for the desired time from the Time-out Chart. The RFC 8-RC will respond in CW with "APTO OK". This command affects both the on-site and remote autopatch.

SETTING CW SPEEDS:

SPEED CHART:	0 = 10 WPM	3 = 25 WPM
	1 = 15 WPM	4 = 30 WPM
	2 = 20 WPM	

ID SPEED (Default 20 WPM)

To set the ID speed enter '*7416x' where 'x' = 0-4 for the desired speed from the Speed Chart. The RFC 8-RC will respond in CW with "IS OK".

(NOTE: ID's are limited to 20 WPM. See FCC Rules Part 97.84.)

COMMAND ACKNOWLEDGMENT SPEED (Default 20 WPM)

To set the speed of the command acknowledgments enter '*7417x' where 'x' = 0-4 for the desired speed from the Speed Chart. The RFC 8-RC will respond in CW with "AS OK".

LINK TIMING (Default Simplex)

This command selects the timing parameters for a simplex or duplex link channel. For simplex operation enter '*74180'. For duplex operation enter '*74181'. The controller will respond in CW with "LNK".

ID TIMING (Default-No delay)

This command is used to delay the ID by 10 seconds when the system is connected to another repeater via the link or remote base channels. The purpose of this is to prevent both repeaters from identifying simultaneously when first keyed up. For normal operation enter '*74190'. For delayed operation enter '*74191'. The controller will respond with "IDI".

COMMAND PREFIXES

To set the command prefixes enter the code for the desired prefix, unkey, wait for acknowledgment, then enter the new prefix. Prefixes must be from one to four digits in length and must NOT contain the sequence 'AC' nor may they contain the '#' except as the first digit. If the new prefix is not entered within ten seconds you will have to start over. Be sure you don't duplicate prefixes.

CODE	RESPONSE	PURPOSE	DEFAULT
<u>System MODE 1 Commands:</u>			
*40900	MID OK	Set Manual ID Code	54
*40901	RPT OK	Set Repeater Command Prefix	2587
*40902	LNK OK	Set Link Command Prefix	321
*40903	RMT OK	Set Remote Base Command Prefix	654
*40904	AUX OK	Set Auxiliary Control Command Prefix	47
*40905	COP OK	Set Control Operator Command Prefix	852
*40906	TP OK	Set TT Access Command Prefix	55
*40907	PS OK	Set Preset Mode Prefix	08

System MODE 2 Commands:

*40908	PA OK	Set Autopatch Access Code	*841
*40909	PD OK	Set Autopatch Disconnect Code	#8
*40910	RPA OK	Set Remote Autopatch Access Code	*89
*40911	RPD OK	Set Remote Autopatch Disconnect Code	#9
*40912	AD OK	Set Autopatch Autodial Prefix	*
*40913	OL OK	Set Dialing Prefix	-
*40914	CH OK	Set Channel Select Prefix	82
*40915	CK OK	Set Remote Base Freq. Check Code	36
*40916	RBF OK	Set Remote Base Freq. Command Prefix	58
*40917	MEM OK	Set Memory Command Prefix	14
*40918	ST OK	Set CTCSS Prefix	21
*40919	RBS OK	Set Remote Base Select Prefix	53

PRESET PARAMETERS

You have the ability to setup three preset modes of operation. To load the operating parameters for a particular operating mode, setup the repeater, link, remote base, auxiliary outputs, timers, tone pitches, etc. the way you want for that mode and then enter '*489x' where x = 0-9 for the desired mode to store the preset mode in memory. After the Presets are loaded, all you need do is enter one command to change the system configuration for a particular type of operation.

NOTE: Preset #0 is used by the Remote Autopatch System.

SYSTEM OPERATING MODE (Default MODE 1)

For MODE 1 operation of the RFC 8-RC enter '*8101'. The controller will respond with "MD 1 OK". For Extended operation, MODE 2, with the optional accessory boards enter '*8102'. The RFC 8-RC will respond with "MD 2 OK". When powered up, the RFC 8-RC normally checks for each optional accessory and selects the correct mode.

NOTE: The following commands require the RFC 8-RC to be in MODE 2.

NOTE: This command requires least one RFC 8-RB Remote Base Board.

MEMORY SET - System MODE 2

This command is used to store the current remote base #, frequency, offset and sub-audible tone into one of the ten memory channels. To program a channel enter '*963x' where 'x' = 0-9 for the desired channel. The current remote base #, frequency, offset and sub-audible tone, if any, will be stored in the desired memory channel. The RFC 8-RC will respond in CW with "M #" where '#' is the channel number (0-9).

AUTODIAL NUMBERS - System MODE 2

NOTE: These commands requires the presence of the RFC 8-AP Autopatch.

To program the telephone numbers in the autodial memory, enter '*586xx' where 'xx' = 00 to 99 for the particular memory you wish to program. The controller will respond with "AD xx OK". After the acknowledgment enter the complete telephone number. If the number has been accepted the RFC 8-RC will respond with 'dit-dit'.

DIALING PREFIX - System MODE 2

This command is used to enter a dialing prefix which is added to the beginning of all phone numbers entered manually or resident in the autodial memory. This feature is useful if your telephone line requires an entry to access an outside line. It will also allow four digit dialing if all phone numbers in your area contain the same prefix. To enter a dialing prefix, enter '*40913'. The controller will respond with "OL OK". After the acknowledgment, enter the desired dialing prefix. If you do not wish to have a dialing prefix, enter '*' instead of a numerical prefix.

REMOTE AUTOPATCH

The RFC 8-RC, with the addition of the RFC 8-RP, will automatically send the Access, Autodial, Redial, and Disconnect commands to a remote autopatch. To set the Remote Autopatch Access Code, as sent by the RFC 8-RC, enter '*40920'. After the acknowledge, "RAC OK", enter the access code. To set the Remote Autopatch Disconnect Code, as sent by the RFC 8-RC, enter '*40921'. After the acknowledge, "RDC OK", enter the disconnect code. To set the Remote Autopatch Autodial Access Code, as sent by the RFC 8-RC, enter '*40922'. After the message, "RAD OK", enter the required autodial prefix. NOTE: The same conditions concerning timing of these entries are the same as setting the command prefixes.

LOCK CONTROLLER

To lock the controller enter '*#'. The RFC 8-RC will respond in CW with "LOCK".

INITIALIZE

This command should be used ONLY if the controller is not functioning properly. This command will erase all values in the EEPROM, including the ID call sign, and set them to the default values. To initialize the RFC 8-RC, enter '0', your Unlock Code, and '0'. Enter all 11 digits as one sequence. The RFC 8-RC will reload the EEPROM with the default values and restart itself. If the system has recovered the repeater should come on the air and ID. If this command does not solve the malfunction you more than likely have a hardware problem.

CONTROL OPERATOR COMMANDS

Control Operator Commands are made up of the Control Operator Prefix followed by a three digit code, except for the following three commands, Repeater Control, System Reset and Preset Mode commands. They have their own prefixes. Each Control Operator command is separately described below. See page A-4 for summary of commands.

REPEATER CONTROL: (Default 2587)

On/Off

The system may be shut off by entering the Repeater Control Prefix followed by a '0'. The RFC 8-RC will respond in CW with "OFF" and immediately shut down. To activate the system, enter the Repeater Control Prefix followed by a '1'. The RFC 8-RC will respond in CW with "ON".

CTCSS Tone Access

To place the system in Tone Access, enter the Repeater Control Prefix followed by a '2'. The RFC 8-RC will respond with "TS".

DUPLEX CONTROL-LINK MODES (Carrier/Tone)

These modes are identical to normal repeater operation except the repeater transmitter will be turned OFF when there is a signal present on the repeater receiver. This type of operation is used to prevent repeater receiver audio from being repeated out the repeater transmitter or when the RFC 8-RC is used at the telephone line end of a remote autopatch link.

Duplex Control-Link Carrier Access

To enter this mode, with Carrier Access, enter the Repeater Control Prefix followed by a '3'. The RFC 8-RC will respond with "DC".

Duplex Control-Link CTCSS Tone Access

To use this mode, with Tone Access, enter the Repeater Control Prefix followed by a '4'. The controller will respond with "DC TS".

SYSTEM RESET (Default AC)

To force a hardware reset enter 'AC'. After a few seconds a hardware reset will occur. None of the previously programmed parameters will be lost

NOTE: This requires the use of 16 button Touch-Pad.

NOTE: Control Operator Prefix Default is 852

COURTESY TONE

The courtesy tone system may be turned off by entering the Control Operator Prefix followed by '000'. The RFC 8-RC will respond in CW with "CT OFF". To enable the courtesy tone system enter the Control Operator Prefix followed by '001'. The RFC 8-RC will respond in CW with "CT ON".

ALARM SYSTEM

The Alarm System, when enabled, will send "A" immediately when the receiver squelch closes to signal an alarm condition. To disable the alarm enter the Control Operator Prefix followed by '010'. The RFC 8-RC will respond in CW with "ARM OFF". To enable the alarm enter the Control Operator Prefix followed by '011'. The RFC 8-RC will respond in CW with "ARM ON".

PRIVACY TONE

This command is used to turn the Privacy Tone off and on. To turn the tone off enter the Control Operator Prefix followed by '020'. The RFC 8-RC will respond in CW with "PT OFF". To turn on the Privacy Tone enter the Control Operator Prefix followed by '021'. The RFC 8-RC will respond in CW with "PT ON".

REPEATER TIME-OUT

The repeater time-out timer may be enabled or disabled using this command. To disable the repeater time-out timer enter the Control Operator Prefix followed by '030'. The RFC 8-RC will respond in CW with "RTO OFF". To enable the repeater time-out timer enter the Control Operator Prefix followed by '031'. The RFC 8-RC will respond in CW with "RTO ON".

LINK TIME-OUT

The link time-out timer may be enabled or disabled using this command. To disable the link time-out timer enter the Control Operator Prefix followed by '040'. The RFC 8-RC will respond in CW with "LTO OFF". To enable the link time-out timer enter the Control Operator Prefix followed by '041'. The RFC 8-RC will respond in CW with "LTO ON".

REMOTE BASE TIME-OUT

The remote base time-out timer may be enabled or disabled using this command. To disable the remote base time-out timer enter the Control Operator Prefix followed by '050'. The RFC 8-RC will respond in CW with "RBTO OFF". To enable the remote base time-out timer enter the Control Operator Prefix followed by '051'. The RFC 8-RC will respond in CW with "RBTO ON".

TOUCH-PAD (T-P) ACCESS MODE

This mode requires a user to enter a code from a Touch Pad to activate the system in repeater mode. The repeater will then operate in a normal manner, resetting after a period of inactivity. This mode may be used to prevent unwanted signals from activating the system. To disable this mode enter the Control Operator Prefix followed by '060'. The RFC 8-RC will respond in CW with "TP OFF". To enter this operating mode enter the Control Operator Prefix followed by '061'. The RFC 8-RC will respond in CW with "TP ON".

NOTE: Only access through the repeater receiver is affected.

IDENTIFIER

This command is used to enable or disable the ID'er. To turn off the ID'er enter the Control Operator Prefix followed by '070'. The RFC 8-RC will respond in CW with "ID 0". To enable the ID'er, repeater transmitter only, enter the Control Operator Prefix followed by '071'. The RFC 8-RC will respond in CW with "ID 1". To allow the ID'er to activate the link transmitter, if enabled, enter the Control Operator Prefix followed by '072'. The RFC 8-RC will respond with "ID 2". To allow the ID'er to activate the remote base transmitter, if enabled, enter the Control Operator Prefix followed by '073'. The controller will respond with "ID 3". To allow the ID'er to activate the link and remote base transmitters, if enabled, enter the Control Operator Prefix followed by '074'. The RFC 8-RC will respond with "ID 4".

USER COMMANDS

This command is used to enable or disable the User Commands. To disable the User Commands enter the Control Operator Prefix followed by '080'. The RFC 8-RC will respond in CW with "USR OFF". To enable the User Commands enter the Control Operator Prefix followed by '081'. The RFC 8-RC will respond in CW with "USR ON".

LINK CONFIGURATION

This command is used to select one of two configurations for the link channel.

Option #1 will not allow the link and remote base to be cross-connected. The link and remote base will be accessible only through the repeater receiver. This option is selected by entering the Control Operator Prefix followed by '090'. The controller will respond in CW with "CC OFF".

Option #2 allows the link and remote base to be cross-connected. To select this option enter the Control Operator Prefix followed by '091'. The controller will respond in CW with "CC ON".

NOTE: If the link or the remote base is connected to a repeater that has a hang time delay and both the link and remote base radios are simplex, this mode is not recommended.

ACCESS (Carrier or CTCSS Tone)

This command is used to select one of four access modes for commanding the controller.

Access Mode #1 allows Carrier Access for all commands. Select this mode by entering the Control Operator Prefix followed by '101'. The RFC 8-RC will respond with "AM 1".

NOTE:The following requires a CTCSS control signal from the repeater receiver.

Access Mode #2 requires the presence of a CTCSS Tone in order to access any of the Setup Commands. Select this mode by entering the Control Operator Prefix followed by '102'. The RFC 8-RC will respond with "AM 2".

Access Mode #3 requires the presence of a CTCSS Tone in order to access any of the Setup or Control Operator Commands. To select this mode, enter the Control Operator Prefix followed by '103'. The controller will respond with "AM 3".

Access Mode #4 requires the presence of a CTCSS Tone to access any of the commands. To select this mode, enter the Control Operator Prefix followed by '104'. The RFC 8-RC will respond with "AM 4".

LINK ACCESS

This command is used to set the Link Access to Carrier or CTCSS tone. For Carrier access to the link transmitter, enter the Control Operator Prefix Followed by '110'. The RFC 8-RC will respond with "LTA OFF". For CTCSS tone to access the link transmitter, enter the Control Operators Prefix followed by '111'. The RFC 8-RC will respond with "LTA ON"

REMOTE BASE ACCESS

This command is used to set the Remote Base Access to Carrier or CTCSS tone. For Carrier access to the Remote Base transmitter, enter the Control Operator Prefix Followed by '120'. The RFC 8-RC will respond with "RBTA OFF". For CTCSS tone to access the Remote Base transmitter, enter the Control Operators Prefix followed by '121'. The RFC 8-RC will respond with "RBTA ON"

COMMAND ACKNOWLEDGE

This command enables or disables the CW acknowledgments. When the acknowledgments are disabled the RFC 8-RC will send "Dit-Dit" in place of the normal CW message. To disable the CW messages enter the Control Operator Prefix followed by '130'. The RFC 8-RC will respond in CW with "dit-dit". To enable the CW messages enter the Control Op prefix followed by '131'. The RFC 8-RC will respond in CW with "CW ON".



AUXILIARY CONTROL

This command is used to allow the RFC 8-RC to activate the link and/or remote base transmitters during command acknowledgments when commands are being entered via the control receiver input. This is useful when the system is being controlled via a link from a distant system. To disable this function, enter the Control Operator Prefix followed by '140'. The controller will respond with "AXK 0". To send acknowledgments out the link transmitter, enter the Control Operator Prefix followed by '141'. The RFC 8-RC will respond with "AXK 1". To send acknowledgments out the remote base transmitter, enter the Control Operator Prefix followed by '142'. The RFC 8-RC will respond with "AXK 2". To send acknowledgments out the link and remote base transmitters, enter the Control Operator Prefix followed by '143'. The controller will respond with "AXK 3".

NOTE: The following commands require the RFC 8-AP Autopatch.

AUTOPATCH ENABLE - System MODE 2

This command will enable or disable the User Autopatch Access. To disable access enter the Control Operator prefix followed by '150'. The RFC 8-RC will respond in CW with "AP OFF". To allow access enter the Control Operator prefix followed by '151'. The RFC 8-RC will respond in CW with "AP ON". To allow access only when a CTCSS Tone is present, enter the Control Operator Prefix followed by '152'. The RFC 8-RC will respond with "AP TA".

NOTE: This command has no effect on the RFC 8-RP.

AUTOPATCH-CONTROL OP ACCESS - System MODE 2

This command will allow the control operators to access the autopatch even if the patch is disabled. This command may also be used to check the telephone line for dial tone as it will not be heard at the beginning of normal autopatch operation. For access enter the Control Operator Prefix followed by '161'. The controller will respond with "OH" and connect to the phone line. To disconnect the patch, enter the Patch Disconnect Code. The RFC 8-RC will respond with "DN".

NOTE: This command has no effect on the RFC 8-RP.

AUTOPATCH ACTIVITY TIMER - System MODE 2

This command is used to enable or disable the autopatch activity timer. To disable the timer enter the Control Operator Prefix followed by '170'. The RFC 8-RC will respond in CW with "APTO OFF". To enable the timer enter the Control Operator Prefix followed by '171'. The RFC 8-RC will respond in CW with "APTO ON".

NOTE: This command affects both the RFC 8-AP and RFC 8-RP.

This command is used to restrict autopatch calls to the local calling area. To restrict calls enter the Control Operator Prefix followed by '180'. The RFC 8-RC will respond in CW with "TC OFF". To allow long distance dialing enter the Control Operator Prefix followed by '181'. The RFC 8-RC will respond in CW with "TC ON".

NOTE: This command has no affect on the RFC 8-RP.

NOTE: The following commands require the presence of the RFC 8-AP or RFC 8-RP.

PRIVATE PATCH - System MODE 2

There are three different types of operation available for the autopatch. In normal operation, all audio from the repeater receiver will be passed on to the repeater transmitter. Select this mode by entering the Control Operator Prefix followed by '190'. The RFC 8-RC will respond with "PP OFF".

Private Patch Mode #1 inhibits all audio from the repeater receiver from being passed on to the repeater transmitter. Only audio from the telephone line will be heard over the repeater transmitter. Select this mode by entering the Control Operator Prefix followed by '191'. The controller will respond with "PP ON".

Private Patch Mode #2 is the same as Mode #1 except that when the repeater receiver is active the DTMF Privacy Tone will be sent over the repeater transmitter. This mode is selected by entering the Control Operator Prefix followed by '192'. The RFC 8-RC will respond with "PPT ON".

REMOTE AUTOPATCH

This command is used to enable and disable access to a remote autopatch. To disable access, enter the Control Operator Prefix followed by '200'. The controller will respond with "RP OFF". To allow access, enter the Control Operator Prefix followed by '201'. The RFC 8-RC will respond with "RP ON".

See page A-6 for summary of commands.

MANUAL ID (Default 54)

You may manually trigger the ID'er by entering the Manual ID Command. This command will function even if the ID'er is disabled.

T-P (Touch pad) REPEATER ACCESS (Default 55)

When this mode is selected the repeater will not repeat until the T-P Access Command Prefix followed by a '1' is entered. The RFC 8-RC will respond in CW with "UP". Normal repeater operation will take place until there is no activity for a predetermined time or a user takes the system down by entering the T-P Access Command Prefix followed by a '0'. The RFC 8-RC will respond in CW with "DN" and go off the air. Note that this feature only affects access through the repeater receiver. Signals coming in on the link or remote base receivers, if enabled, will still play out through the repeater transmitter.

AUXILIARY OUTPUTS (Default 47)

These outputs are available directly when operating in MODE 1. In MODE 2 the use of these outputs requires the installation of an external decoder to recover the encoded data. To set or reset the eight auxiliary functions enter the Auxiliary Control Prefix followed by the line # (1-8) and a '0' to turn off or a '1' to turn on. The RFC 8-RC will respond in CW with "F" followed by the line #, and "OFF" or "ON".

To check the status of these outputs enter the Auxiliary Control Prefix followed by "0". The RFC 8-RC will respond in CW with a line number if that particular line is turned on. If all Aux Outputs are off, the RFC 8-RC will respond with "0".

PRESET MODES (Default 08)

To select one of the ten Preset Operating Modes enter the Preset prefix followed by '0-9'. The RFC 8-RC will respond in CW with "PS #" where "#" is the mode number and then configure the current operating parameters to the desired mode.

LINK FUNCTIONS

(Default 321)

There are five link commands. Each is preceded by the Link Command Prefix. The last digit may be a '0', '1', '2', '3', or '4'. The '0', example '3210', disables the link entirely and is acknowledged in CW with "LNK OFF". The '1', example '3211', enables only the link receiver so that you may monitor the link channel but not bother users on the other end. This command is acknowledged in CW with "LNK RX". The '2', example '3212', enables only the link transmitter. This command is useful for certain types of operation and testing a path. This command is acknowledged in CW with "LNK TX". The '3', example '321', enables both the receiver and transmitter of the link allowing conversations to be passed both ways. This command is acknowledged in CW with "LNK ON". The '4', example '3214', will report on the status of the link.

When the link transmitter is enabled, a two-tone beep will be heard to notify users the link transmitter is on.

REMOTE BASE FUNCTIONS

(Default 654)

If operating in MODE 1 you are limited to a single frequency remote base. Commands are the same as the link but are preceded by the Remote Base Command Prefix and the CW response will contain "RMT" in place of "LNK".

When the remote base transmitter is enabled, a two-tone beep will be heard to notify users the remote base transmitter is on.

AUTOPATCH

AUTOPATCH - System MODE 2 Default: Access code *841
Disconnect code #8

To access the autopatch enter the Autopatch Access Code. If the patch is enabled the RFC 8-RC will respond in CW with "AP". After the controller sends "AP", enter the telephone number. When you unkey after entering the number, the RFC 8-RC will connect to the telephone line and redial the number with regenerated tones. You must begin dialing your number within ten seconds or the autopatch will disconnect. After you have dialed your number the autopatch timer will be set to the value programmed with the Setup Commands. This timer will reset each time you make a transmission. To shut off the autopatch enter the Autopatch Disconnect Code. The RFC 8-RC will respond with "DN" and disconnect.

REDIAL - System MODE 2 Default: Redial *841*
Disconnect #8

To redial the last number dialed on the autopatch, enter the Autopatch Access Code followed by '*'. Enter this as one command. The RFC 8-RC will respond with "RD" and automatically dial the number. Disconnecting when the call is completed is the same as normal autopatch operation.

AUTODIAL - System MODE 2 Default: Autodial Prefix *
Disconnect #8

To dial a number contained in the autodial memory enter the Autodial Prefix followed by 'xx' where 'xx = 00 - 99' for the desired memory location. The controller will respond with "AD xx" and then dial your number for you. Disconnecting when the call is completed is the same as normal autopatch operation.

REMOTE AUTOPATCH Default: Connect code *89
Disconnect code #9)

To access the remote autopatch, enter the Remote Autopatch Connect Code. The controller will send 'dit-dit' and enter the remote patch mode. To disconnect the remote patch enter the Remote Autopatch Disconnect Code. The controller will send 'dit-dit' and return to normal operation. To redial a number on the remote autopatch, enter the Remote Autopatch Access Code followed by '*'. The RFC 8-RC will access the remote autopatch and redial the last number for you. To access the autodialer on the remote autopatch, enter the Remote Autopatch Connect Code followed by '00-99' for the desired autodial location. The RFC 8-RC will send 'dit-dit' and access the remote autodialer.

REMOTE BASE FUNCTIONS

CHANNEL SELECT - System MODE 2 (Default 82)

NOTE: This command requires the presence of the RFC 8-AP Autopatch or the RFC 8-SI.

In the case of a multi-channel crystal link or remote base you may select one of eight channels by entering the Channel Prefix followed by the desired channel number (1-8). The RFC 8-RC will respond in CW with "CH #" where "#" is the channel number. To check which channel is currently selected, enter the Channel Select Prefix followed by '0'. The RFC 8-RC will respond with "CH #" where "#" is the channel currently selected.

NOTE: The following commands require the presence of at least one RFC 8-RB Remote Base Interface.

REMOTE BASE FREQUENCY - System MODE 2 (Default 58)

When operating in MODE 2 you have the choice of a crystal controlled (8 channels) or a fully synthesized remote. (An external decoder is required to recover the encoded data for a crystal or synthesized remote.)

For the synthesized remote the frequency is set by entering the Frequency Set Prefix followed by the MHz, 100 KHz, 10 KHz, 1 KHz and offset. For offset, 0 = simplex, 1 = minus, and 2 = plus. The RFC 8-RC will output the new frequency and then read back the Remote Base #, Frequency, and Offset back in CW. If the CTCSS encoder is on, the Offset response will be "8", "9", or "A" instead of "0", "1", or "2".

REMOTE BASE FREQUENCY CHECK - System MODE 2 (Default 36)

To check the current frequency of the remote base enter the Frequency Check Command. The current Remote Base #, Frequency, and Offset will be read back in CW. If the CTCSS encoder is on, the Offset response will be "8", "9", or "A" instead of "0", "1", or "2".

CTCSS TONE ENCODE - System MODE 2 (Default 21)

You have the ability to select one of thirty two sub-audible tones. To program the encoder enter the CTCSS Prefix followed by two digits for desired tone (01-32). The RFC 8-RC will respond with "ST ###" where "###" is the tone number. To turn off the encoded enter the CTCSS Prefix followed by '00'. The response will be "ST OFF". To check which CTCSS tone is currently selected, enter the CTCSS Prefix followed by '0'. The RFC 8-RC will respond with "ST #" if a tone is selected or with "ST OFF" if no tone is selected.

REMOTE BASE MEMORY CHANNELS - System MODE 2

(Default 14)

The RFC 8-RC also provides for ten channels of memory for the remote base. Each memory channel contains the Remote Base #, Frequency, and CTCSS tone. To select one of these memories enter the Memory Prefix followed by the desired memory channel number (0-9). The RFC 8-RC will respond with "M #" where "#" is the memory number.

MULTIPLE REMOTE BASES - System MODE 2

(Default 53)

When you are using multiple remotes you may choose one from up to eight to be on line at any one time. To select a remote enter the Remote Base Select Prefix followed by the remote # (1-8). The RFC 8-RC will respond with "RB #" where "#" is the current remote. To check which remote base is currently selected, enter the Remote Base Select Prefix followed by '0'. The RFC 8-RC will respond with "RB #" where "#" is the remote base currently selected.

BASIC CIRCUIT DESCRIPTION

The various receiver audios go to a buffer, U8. The outputs of U8 are connected to U10. U10 is a multiplexer, it selects which of the receive audios will go to the transmitter audio output terminal and to the DTMF decoder. The output of U10 goes to the AUX OUTPUT PIN, Q2, U11, and U9C. Q2 is an FET switch which mutes transmitter audio when DTMF tones are being received. The AUX audio is not muted. U9D is the mixer for the transmitter audio. U11 is the DTMF decoder. It receives the tones and decodes them into a digital format.

The various COS inputs go to U5. U5 is an inverting buffer that isolates the COS inputs from the microprocessor circuitry.

Q3, Q4, and Q5 are the drivers for the PTT outputs. These outputs are controlled by the microprocessor to select which transmitter is turned on at any one time.

Microcomputer:

A detailed explanation of the Microcomputer is beyond the scope of this manual. Below is a brief description of the Microcomputer operation.

U1 is an 8085A microprocessor. It is the heart of the RFC 8-RC. In conjunction with U2, U3, U13, U14, and U15 form the Microcomputer that controls the operation of the RFC 8-RC.

The operating instructions (software) is factory programmed into U2. U2 is a 16K byte EPROM. The command codes and other user programmable operating parameters are stored in U3. U3 is 2K byte EEPROM which retains its memory even when the power is removed.

U3 is a multipurpose IC. Besides handling all the input and output, it contains the tone generator and 256 bytes of RAM.

U4 is used to generate sine wave tones for the RFC 8-RC. Its output goes to R15, TONE LEVEL ADJUST, then to a low pass filter, U9A, where it is filtered and then to U9D where it is mixed with the transmitter audio.

U6 and U7 are connected as a "Watchdog Timer". This timer is normally supplied with reset pulses when the RFC 8-RC is operating properly. If the RFC 8-RC malfunctions, the reset pulses will cease and the timer will begin to operate. When the terminal count is reached, U6 will force a hardware reset to the Microcomputer.

U12 is a darlington driver used as a buffer for the eight auxiliary output lines..

SUMMARY OF COMMANDS

SETUP COMMANDS

UNLOCK CODE _____

CODE RESPONSE

Programming the ID Message

*8090	ID OK	Program ID Message			
	CW Chart:	0 - 00	9 - 09	I - 18	R - 27
		1 - 01	A - 10	J - 19	S - 28
		2 - 02	B - 11	K - 20	T - 29
		3 - 03	C - 12	L - 21	U - 30
		4 - 04	D - 13	M - 22	V - 31
		5 - 05	E - 14	N - 23	W - 32
		6 - 06	F - 15	O - 24	X - 33
		7 - 07	G - 16	P - 25	Y - 34
		8 - 08	H - 17	Q - 26	Z - 35

Setting the Tone Frequencies (x = 0-9)

*4560x	IDT OK	Set ID Pitch
*4561x	CT1 OK	Set Repeater Courtesy Tone
*4562x	CT2 OK	Set Link Courtesy Tone
*4563x	CT3 OK	Set Remote Base Courtesy Tone
*4564x	ACK OK	Set Command Acknowledgment Tone
*4565x	PT OK	Set Privacy Tone

TONE CHART:	0 = 400 Hz	5 = 1225 Hz
	1 = 500 Hz	6 = 1530 Hz
	2 = 625 Hz	7 = 1910 Hz
	3 = 780 Hz	8 = 2375 Hz
	4 = 975 Hz	9 = 2980 Hz

Setting the Hang Timers (x = 0-9)

*7410x	HT OK	Set Repeater Hang Time
*7411x	LT OK	Set Link Hang Time
*7412x	RT OK	Set Remote Base Hang Time

HANG TIME CHART:	0 = .05 Sec	5 = 2.0 Sec
	1 = .25 Sec	6 = 2.5 Sec
	2 = .50 Sec	7 = 3.0 Sec
	3 = 1.00 Sec	8 = 3.5 Sec
	4 = 1.50 Sec	9 = 4.0 Sec

Setting the Time-out Timers (x = 0-5)

*7413x	TO OK	Set Repeater Timer
*7414x	ATO OK	Set T-P Access Time-out
*7415x	APTO OK	Set Autopatch Activity Timer

TIME-OUT CHART:

0 = .5 Min	3 = 2.0 Min
1 = 1.0 Min	4 = 2.5 Min
2 = 1.5 Min	5 = 3.0 Min

Setting CW Speeds (x = 0-4)

*7416x	IS OK	Set ID Speed
*7417x	AS OK	Set Acknowledgment Speed

SPEED CHART:

0 = 10 WPM	3 = 25 WPM
1 = 15 WPM	4 = 30 WPM
2 = 20 WPM	

Link Selection/Timing

*74180	LNK OK	Select Simplex Link
*74181	LNK OK	Select Duplex Link

		ID Timing
*74190	IDI OK	Normal
*74191	IDI OK	10 Second Delay

Preset Modes

*489x	PSx OK	Setup Preset Mode #x (x=0-9)
-------	--------	------------------------------

Setting the Operating Mode

*8101	MD 1 OK	Select Mode #1 (BASIC Operation)
*8102	MD 2 OK	Select Mode #2 (EXPANDED Operation)

 Programming the Command Prefixes

MODE 1 Commands:

*40900	MID OK	Set Manual ID Code	54
*40901	RPT OK	Set Repeater Command Prefix	2587
*40902	LNK OK	Set Link Command Prefix	321
*40903	RMT OK	Set Remote Base Command Prefix	654
*40904	AUX OK	Set Auxiliary Control Command Prefix	47
*40905	COP OK	Set Control Operator Command Prefix	852
*40906	TP OK	Set TT Access Command Prefix	55
*40907	PS OK	Set Preset Mode Prefix	08

MODE 2 Commands:

*40908	PA OK	Set Autopatch Access Code	*841
*40909	PD OK	Set Autopatch Disconnect Code	#8
*40910	RPA OK	Set Remote Autopatch Access Code	*89
*40911	RPD OK	Set Remote Autopatch Disconnect Code	#9
*40912	AD OK	Set Autopatch Autodial Prefix	*
*40913	OL OK	Set Dialing Prefix	-
*40914	CH OK	Set Channel Select Prefix	82
*40915	CK OK	Set Remote Base Freq. Check Code	36
*40916	RBF OK	Set Remote Base Freq. Command Prefix	58
*40917	MEM OK	Set Memory Command Prefix	14
*40918	ST OK	Set CTCSS Prefix	21
*40919	RBS OK	Set Remote Base Select Prefix	53
*40920	RAC OK	Set Remote Patch Access (System)	*
*40921	RDC OK	Set Remote Patch Disconnect (System)	#
*40922	RAD OK	Set Remote Patch Autodial (System)	*

 Locking the RFC 8-RC

LOCK Secure Controller

 Initializing the RFC 8-RC

0 UNLOCK CODE 0 Initialize RFC 8-RC (Use ONLY in case of malfunction)

NOTE: The following commands are used in MODE 2 ONLY

 Programming the Memory Channels (x = 0-9)

*963x M x Program Memory Channel (x = Channel #)

 Programming the Autodial Numbers (xx = 01-50)

*586xx AD xx Program Autodial Number (xx = 00-99)

CONTROL OPERATOR COMMANDS

CODE	RESPONSE	FUNCTION

System Reset		
AC		Reset Microprocessor

(xx = Repeater Control Prefix)		
xx0	OFF	System Off
xx1	ON	System On - Carrier Access
xx2	TS	System On - Tone Access
xx3	DC	System in Duplex Control Mode
xx4	DC TS	System in Tone Access Duplex Control Mode

Control Operator Commands		
(xx = Control Operator Prefix)		
xx000	CT OFF	Courtesy Tones Off
xx001	CT ON	" " On
xx010	ARM OFF	Alarm Off
xx011	ARM ON	" On
xx020	PT OFF	Privacy Tone Off
xx021	PT ON	" " On
xx030	RTO OFF	Repeater Time-out Off
xx031	RTO ON	" " On
xx040	LTO OFF	Link Time-out Off
xx041	LTO ON	" " On
xx050	RBTO OFF	Remote Base Time-out Off
xx051	RBTO ON	" " " On
xx060	TP OFF	T-P Access Mode Off
xx061	TP ON	" " " On
xx070	ID OFF	ID'er Off
xx071	ID ON	" Repeater Only
xx072	ID 2	" Repeater/Link
xx073	ID 3	" Repeater/Remote Base
xx074	ID 4	" Repeater/Link/Remote Base
xx080	USR OFF	User Commands Off
xx081	USR ON	" " On
xx090	CC OFF	Link Configuration #1 (Cross-connect OFF)
xx091	CC ON	" " #2 (" " ON)

CODE	RESPONSE	FUNCTION	CODE
xx101	AM 0	Access Mode #1 (Carrier for all commands)	
xx102	AM 1	Access Mode #2 (CTCSS required for Setup Commands)	
xx103	AM 2	Access Mode #3 (CTCSS required for Control Operator/Setup Commands)	
xx104	AM 3	Access Mode #4 (CTCSS required for all commands)	
xx110	LTA OFF	Link Transmitter-Carrier Access	
xx111	LTA ON	" " -CTCSS ACCESS	
xx120	RBTA OFF	Remote Base Transmitter-Carrier Access	
xx121	RBTA ON	" " " -CTCSS Access	
xx130	Dit-dit	CW Acknowledgments Off	
xx131	CW ON	" " " On	
		Control receiver	
xx140	AXK 0	CW Acknowledgments None	
xx141	AXK 1	" " " Repeater/Link	
xx142	AXK 2	" " " Repeater/Remote Base	
xx143	AXK 3	" " " Repeater/Link/Remote Base	
xx150	AP OFF	Autopatch Off	
xx151	AP ON	" On	
xx152	AP TS	" CTCSS Access	
xx161	OH	" Off-Hook	
xx170	APTO OFF	Autopatch Activity Timer Off	
xx171	APTO ON	" " " On	
xx180	TC OFF	Toll Call Access Off	
xx181	TC ON	" " " On	
xx190	PP OFF	Autopatch in Normal Mode	
xx191	PP ON	Autopatch in Private Mode (Silent)	
xx192	PPT ON	Autopatch in Private Mode (Privacy Tone)	
xx200	RP OFF	Remote Patch Disable	
xx201	RP ON	" " Enable	
xx202	RPTA	Remote Patch CTCSS Access	

USER COMMANDS

CODE

CODE	RESPONSE		
xx	Call sign	Manual ID	xx = Manual ID Code

T-P Access (xx = T-P Access Prefix)

xx0	UP	TP Access UP
xx1	DN	TP Access DOWN

Auxiliary Outputs (xx = Auxiliary Command Prefix) (y = Line # <1-8>)

xx0	F y OFF	Set Aux Output Line to OFF
xx1	F y ON	Set Aux Output Line to ON
xx0	#	Check Aux Status (# = Activated Outputs)

Preset Operating Modes (xx = Preset Prefix)

xyy	PS y	Select 1 of 10 Preset Operating Modes (y = 0-9)
-----	------	---

Autopatch

xxx	AP	Autopatch Access (xxx = Patch Access Code)
yyy	DN	Autopatch Disconnect (yyy = Patch Dump Code)
xxx*	RD	Autopatch Access - Last # Redial

Remote Autopatch

xxx	..	Remote Autopatch Access (xxx = Remote Patch Connect Code)
xxx*		Remote Autopatch Redial
xxxxyy		Remote Autopatch Autodial (yy = 00-99)
zzz	..	Remote Autopatch Disconnect (zzz = Remote Patch Disconnect Code)

Link Commands (xx = Link Prefix)

xx0	LNK OFF	Link Off
xx1	LNK RX	Link Receive Only
xx2	LNK TX	Link Transmit Only
xx3	LNK ON	Link Receive/Transmit
xx4	LNK ???	Check Link Status

CODE RESPONSE FUNCTION

Select Link/Remote Base Channel (xx = Channel Select Prefix)

xxY	CH y	Set Link/Remote Base Channel (y = Channel # <1-8>)
xx0	CH #	Check Channel Status (# = Channel Selected)

Remote Base Commands (xx = Remote Base Prefix)

xx0	RMT OFF	Remote Base Off
xx1	RMT RX	Remote Base Receive Only
xx2	RMT TX	Remote Base Transmit Only
xx3	RMT ON	Remote Base Receive/Transmit
xx4	RMT ???	Check Remote Base Status

Set Frequency Command
(xx = Frequency Set Prefix)

Freq Set Remote Base Frequency

xx+(MHz)+(100KHz)+(10KHz)+(1KHz)+(0 = Simplex)
(1 = Minus)
(2 = Plus)

Check Remote Base Frequency

xx	-----	Check Remote Base Frequency	xx = Frequency Check Code
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Select CTCSS Tone (xx = CTCSS Prefix)

xx00	ST OFF	Disable Sub-audible Tone
xxyy	ST yy	Set Sub-audible Tone yy = Tone # (01-32)

Select Remote Base Memory Channel
(xx = Memory Prefix)

xx#	M #	Select Memory Channel (# = Channel # <0-9>)
-----	-----	---

Select Remote Base (xx = Remote Base Select Prefix)

xxY	RB y	Select Remote Base y = Remote Base # (1-8)
xx0	RB #	Check Remote Base Status (# = Remote Base Selected)

DEFAULT SETTINGS

Manual ID	54
Remote Base Frequency Check	36
Repeater Operator Prefix	2587
Link Prefix	321
Remote Base Prefix	654
Remote Base Freq Prefix	58
Auxiliary Prefix	47
Control Operator Prefix	852
Memory Prefix	14
Patch Access Code	*841
Patch Disconnect Code	#8
Autodial Prefix	*
Preset Prefix	08
T-P Access Prefix	55
CTCSS Prefix	21
Remote Base Select Prefix	53
Channel Select Prefix	82
Remote Autopatch Access	*89
Remote Autopatch Disconnect	#9
Remote Autopatch Access (System)	*
Remote Autopatch Autodial (System)	*
Remote Autopatch Disconnect (System)	#

ID Message

CALL/R - Enabled

ID Timing Delay	Normal
Hang Timers	1.5 Second
Time-out Timer	3.0 Minutes - Enabled
Repeater	ON
Link/Remote Base	OFF
Link Configuration	Simplex / Option #1 (Normal)
Courtesy Tones	ON
Alarm	OFF
Privacy Tone	ON
CW Acknowledge	ON
T-P Access	OFF (1 Min)
Access	Option #1 - Carrier Access
Autopatch	ON - Carrier Access
Autopatch Activity Timer	ON (30 Sec)
Toll Call Access	OFF
Private Patch	OFF
Preset Modes	Set to above parameters
System Mode	Mode #1
Auxiliary Outputs	OFF
Autodial Numbers	Blank
Channel Select	Channel #1
CTCSS Encoder	OFF
Remote Base Select	Remote Base #1
Remote Base Memories	xx6.520 Simplex

PIN CONNECTIONS

1 - Audio Ground	19 - N/C
2 - Remote Base Receive Audio	20 - Alarm
3 - Audio +5 volts	21 - Patch-Busy (Autopatch)
4 - Link Receive Audio	22 - Ring Detect
5 - Control Receive Audio	23 - CTCSS Decoder Input
6 - Aux Transmit Audio	24 - Control Receiver COS
7 - Repeater Receive Audio	25 - Remote Base Receiver COS
8 - Tone Out (Autopatch)	26 - Link Receiver COS
9 - Tone In (Autopatch)	27 - Repeater Receiver COS
10 - Transmitter Audio	28 - Digital Ground
11 - Repeater PTT	29 - FREQ Strobe
12 - N/C	30 - AUX Strobe
13 - Link PTT	31 - FREQ Reset
14 - N/C	32 - AP Strobe
15 - Remote Base PTT	33 - Aux Data 8
16 - External Reset	34 - Aux Data 4
17 - N/C	35 - Aux Data 2
18 - Digital +5 volts	36 - Aux Data 1

NOTE: xx designates the pin goes to ground or 0 voltage when activated, or requires a ground to to activate the desired function.

1977-1978		1978-1979	
1	2	3	4
5	6	7	8
9	10	11	12
13	14	15	16
17	18	19	20
21	22	23	24
25	26	27	28
29	30	31	32
33	34	35	36
37	38	39	40
41	42	43	44
45	46	47	48
49	50	51	52
53	54	55	56
57	58	59	60
61	62	63	64
65	66	67	68
69	70	71	72
73	74	75	76
77	78	79	80
81	82	83	84
85	86	87	88
89	90	91	92
93	94	95	96
97	98	99	100

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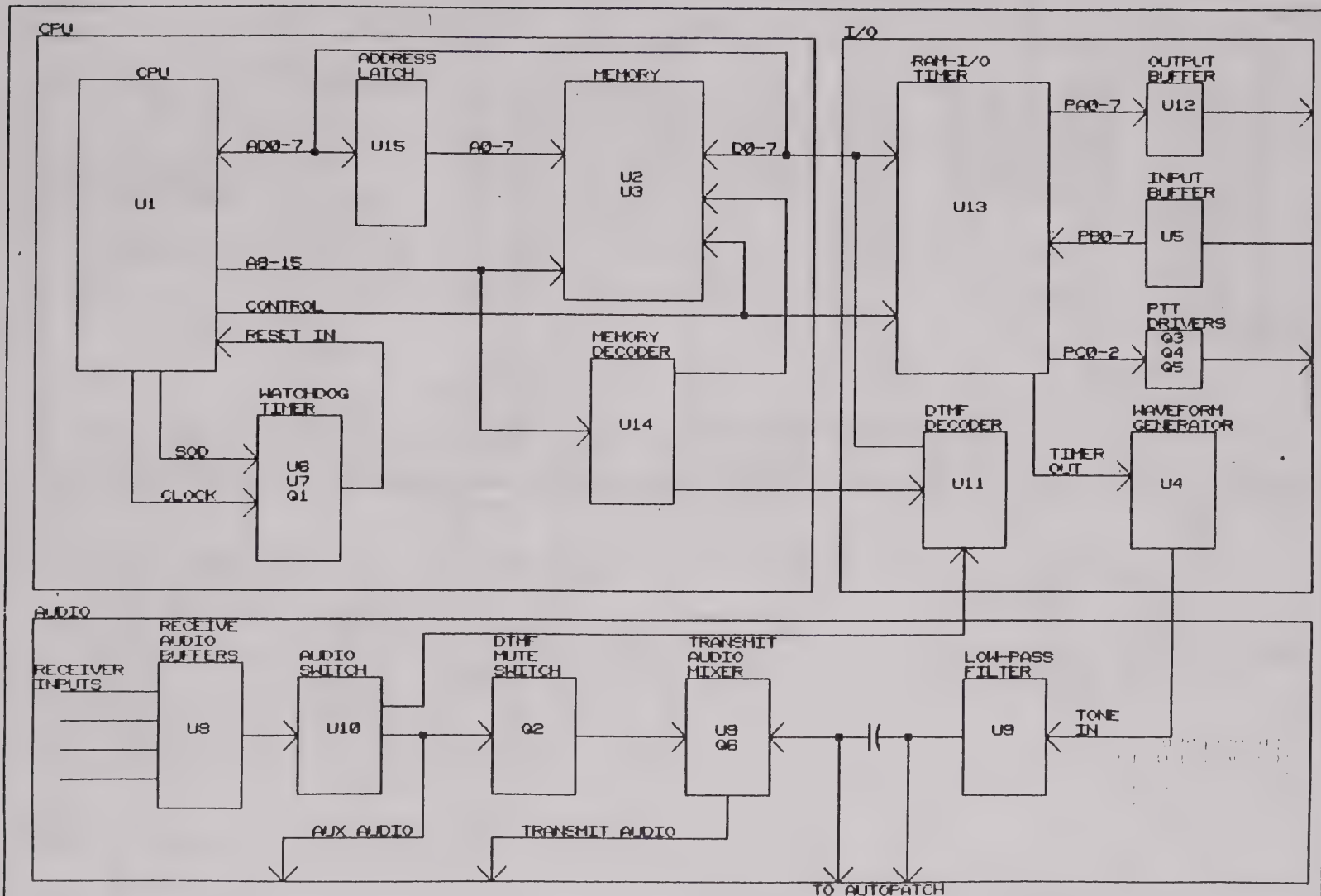
196

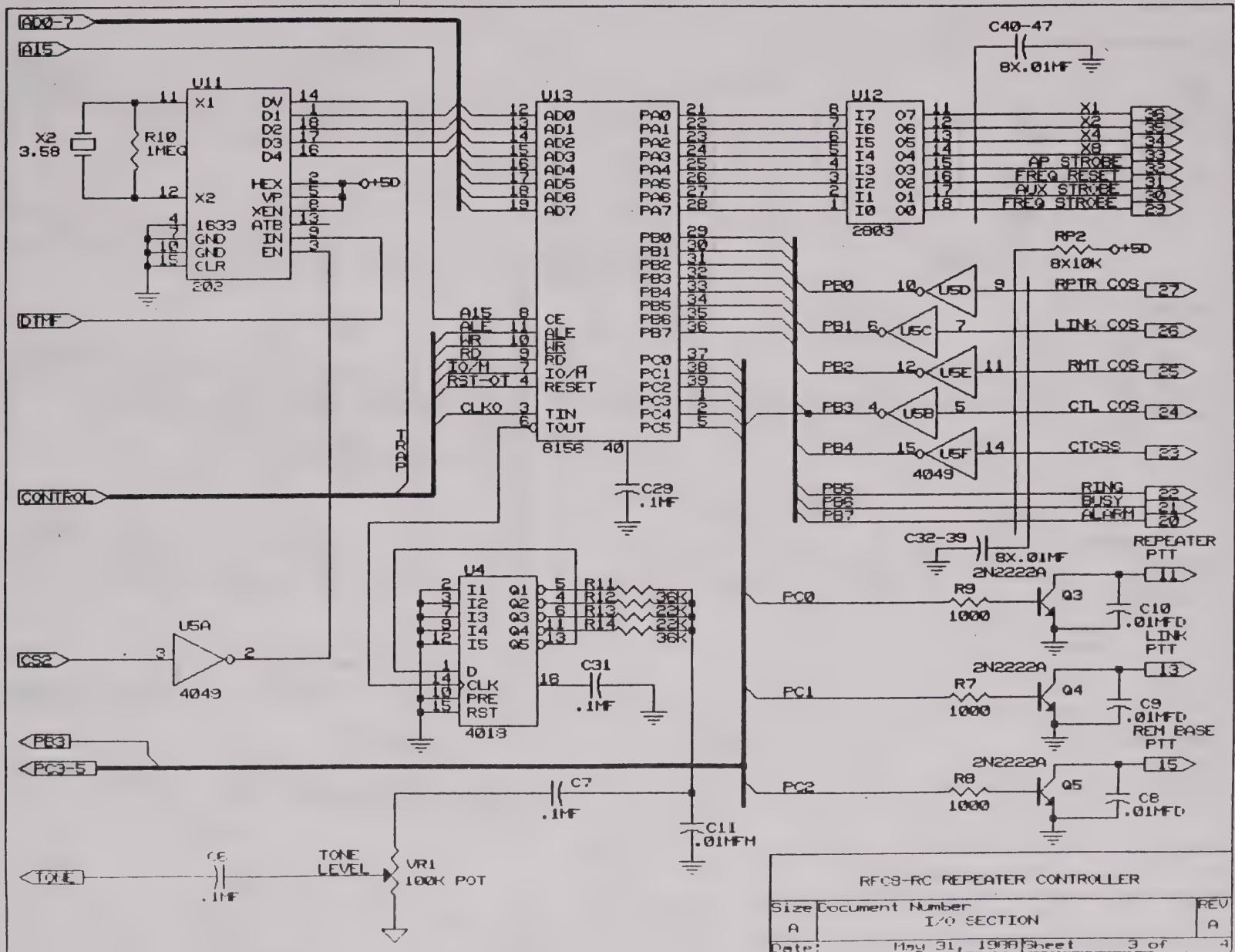
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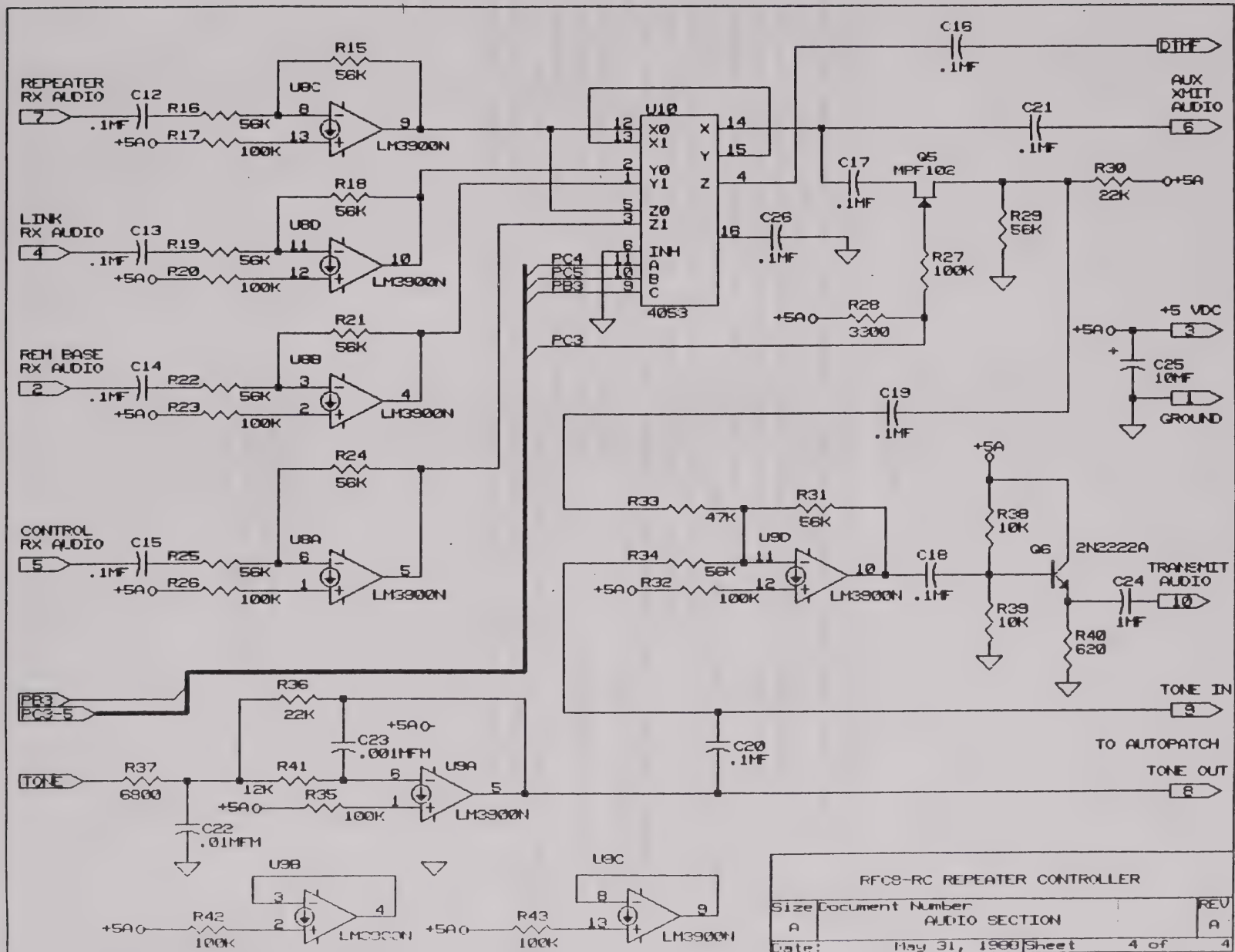
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WARRANTY

RF CONCEPTS, Division of Kantronics, warrants each RFC 8-RC free from defects in material and workmanship under normal use and service for a period of 1 year after the delivery to the ultimate user.

The unit must be returned to the factory, freight prepaid. The warranty card must have been submitted within 15 days after purchase. Any unauthorized repair may void this warranty.

RF CONCEPTS will provide, free of charge, both parts and labor, as necessary, to correct any defect occurring within the warranty period.

This warranty applies to the original owner only.

This warranty applies only to those units that fail during normal operation. Any unit that has been overvoltaged, modified, accidentally damaged or misused will not be covered.

RF CONCEPTS will not assume any responsibility for damage to any radio or accessory connected to this product.

This warranty is in lieu of all other warranties expressed or implied, and no representative or person is authorized to assume for RF Concepts any other liability in connection with the sale of its products.

RF CONCEPTS
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STW
as per Everett
Hawley @ RFE division

RFC 8-AP
AUTOPATCH
INSTRUCTION MANUAL

RF Concepts
Division of Kantronics

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INTRODUCTION	1-1
INSTALLATION/SETUP	2-1
CONTROL OPERATOR COMMANDS	3-1
USER COMMANDS	4-1
PIN CONNECTIONS	A-1
WARRANTY	B-1

WARNING: This product contains static sensitive components.
Take proper precautions to prevent static buildup
while handling.

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INTRODUCTION

The RF Concepts RFC 8-AP Autopatch provides a very powerful interface between the telephone line and a repeater which uses the RFC 8-RC Repeater Controller. All command codes and timers relating to autopatch operation are remotely programmable and are stored in non-volatile memory. In addition to standard autopatch operation, the RFC 8-AP has many advanced features.

The RFC 8-AP features DTMF tone regeneration. What this means is all DTMF tones received from the user will be regenerated with clean, noise-free tones which are then transmitted into the telephone line. This greatly reduces the chances of improper dialing due to a user's signal being noisy, weak, or distorted.

Another advanced feature of the RFC 8-AP is the Autodialer. This Autodialer has the capacity to store up to 100 separate telephone numbers, including area code if required, into non-volatile memory. This allows a user to make an autopatch call by entering as few as three digits. Also, a user may redial the last number dialed by entering as little as two digits.

The RFC 8-AP may be remotely commanded to either allow or disallow toll calls (long distance) from being made through the autopatch. Also provided is an activity timer which may be remotely programmed and switched on or off.

Reverse autopatch as well as remote control via telephone are also provided by the RFC 8-AP. Calls coming in to the RFC 8-AP, from the telephone line, will be answered and the RFC 8-AP will enter the remote command mode. If the caller enters the proper DTMF command, the telephone line will be connected to the repeater and the person on the telephone may then converse with persons on the repeater.

The RFC 8-AP also contains the circuitry for decoding the eight Auxiliary Outputs and the eight Channel Select Lines. Control of the RFC 8-AP requires the use of the Auxiliary Outputs from the RFC 8-RC. These outputs are transferred to RFC 8-AP and are available from this board.

The RFC 8-AP also contains the eight Channel Select line for use with a crystal controlled Link or Remote Base.

INSTALLATION

Installation of the RFC 8-AP Autopatch is relatively simple and straight forward. There are two connections for the telephone line, four connections for power, two connections to the repeater receiver, and fourteen connections to the RFC 8-RC Repeater Controller.

IMPORTANT: It is highly recommended that an FCC approved Telephone Interface Coupler be used between the RFC 8-AP and the telephone lines. This coupler can be obtained from:

MOREY CO.
2659 WISCONSIN AVENUE
DOWNERS GROVE, IL 60515

Order: Model #10X2700 Telephone Interface Coupler

POWER SUPPLY CONNECTIONS

The RFC 8-AP requires +12 volts DC at 000 MA This may be obtained from the repeater or a separate power supply. These two +12 lines should be connected together ONLY at the power source. There are also two separate ground connections required. These grounds should be connected to the corresponding pins on the RFC 8-RC. The pins for the power connections are:

- Pin 1 - Audio Ground (to Pin 1 on RFC 8-RC)
- Pin 3 - Audio +12 (to +12 power source)
- Pin 17 - Digital +12 (to +12 power source)
- Pin 28 - Digital Ground (to Pin 28 on RFC 8-RC)

TELEPHONE LINE CONNECTIONS

The two connections for the telephone are pins 12 and 14. The RFC 8-AP is not polarity sensitive. It is recommended that these two pins be connected to the Telephone Interface Coupler then to a RJ-11 (modular) jack and the telephone line be plugged into the jack and NOT wired directly to the RFC 8-AP.

REPEATER RECEIVER CONNECTIONS

The RFC 8-AP requires two connections to the repeater receiver. These are Repeater Receive Audio and Repeater COS. If you have already installed the RFC 8-RC, these lines are already present on pins 7 and 27 of the RFC 8-RC. If the RFC 8-RC has already been installed, move the wire from pin 7 on the RFC 8-RC (Repeater Receive Audio) to pin 2 of the RFC 8-AP and the wire from pin 27 on the RFC 8-RC (Repeater COS) to pin 19 of the RFC 8-AP. If the RFC 8-RC has not been previously installed, these connections will have to be made to the repeater receiver. See the RFC 8-RC Owner's Manual for more information.

RFC 8-RC CONNECTIONS

There are fourteen connections, plus the ones on page 2-1, to be made to the RFC 8-RC from the RFC 8-AP. These connections are made to the corresponding pins on the RFC 8-RC. These connections are:

<u>RFC 8-AP</u> <u>AUTOPATCH</u>	<u>FUNCTION</u>	<u>RFC 8-RC</u> <u>CONTROLLER</u>
Pin 5	- Control Receiver Audio In	Pin 5
Pin 7	- Repeater Receiver Audio Out	Pin 7
Pin 8	- Tone In	Pin 8
Pin 9	- Tone Out	Pin 9
Pin 21	- Patch Busy	Pin 21
Pin 22	- Ring Detect	Pin 22
Pin 24	- Control COS Out	Pin 24
Pin 27	- Repeater COS Out	Pin 27
Pin 30	- Aux Strobe In	Pin 30
Pin 32	- Autopatch Strobe IN	Pin 32
Pin 33	- Aux Data 3 In	Pin 33
Pin 34	- Aux Data 4 In	Pin 34
Pin 35	- Aux Data 2 In	Pin 35
Pin 36	- Aux Data 1 In	Pin 36

AUX / CHANNEL SELECT OUTPUTS

These outputs are available via the two 9-pin connectors on the end of the board. These outputs go to ground when active (open-collector). The connector nearest the edge of the board contains the eight AUX outputs and the connector nearest the center of the board contains the eight Channel Select Outputs. The pins are numbered in the same direction as the fingers for the edge connector. That is, pin 1 is on the same side of the board as pin 1 on the edge connector and pin 9 is on the side with pin 36. The connections for both the Auxiliary and the Channel Select Outputs are listed below.

Pin 1 - Output #4	Pin 4 - Output #2	Pin 7 - Output #1
Pin 2 - Output #3	Pin 5 - Output #7	Pin 8 - Output #5
Pin 3 - Output #8	Pin 6 - Output #6	Pin 9 - Ground

SETUP

The first step in the setup procedure is to program the various timers and command codes. The procedures for setting these parameters are found in the Setup Commands chapter in the RFC 8-RC manual.

Page 5-3 AUTOPATCH ACTIVITY TIMER

Page 5-4 COMMAND PREFIXES

Page 5-5 AUTODIAL NUMBERS

Page 5-5 DIALING PREFIX

Page 5-6 REMOTE AUTOPATCH

The next step is setting the levels on the RFC 8-AP Autopatch. These levels are preset at the factory and should be tried before any adjustments are made. The three adjustments are DTMF level, receive level, and transmit level.

PRIVATE PATCH - System MODE 2

There are three different types of operation available for the autopatch. In normal operation, all audio from the repeater receiver will be passed on to the repeater transmitter. Select this mode by entering the Control Operator Prefix followed by '190'. The RFC 8-RC will respond with "PP OFF".

Private Patch Mode #1 inhibits all audio from the repeater receiver from being passed on to the repeater transmitter. Only audio from the telephone line will be heard over the repeater transmitter. Select this mode by entering the Control Operator Prefix followed by '191'. The controller will respond with "PP ON".

Private Patch Mode #2 is the same as Mode #1 except that when the repeater receiver is active the DTMF Privacy Tone will be sent over the repeater transmitter. This mode is selected by entering the Control Operator Prefix followed by '192'. The RFC 8-RC will respond with "PPT ON".

REMOTE AUTOPATCH

This command is used to enable and disable access to a remote autopatch. To disable access, enter the Control Operator Prefix followed by '200'. The controller will respond with "RP OFF". To allow access, enter the Control Operator Prefix followed by '201'. The RFC 8-RC will respond with "RP ON".

USER COMMANDS

AUTOPATCH (Default) Access code *841
Disconnect code #8

To access the autopatch enter the Autopatch Access Code. If the patch is enabled the RFC 8-RC will respond in CW with "AP". After the controller sends "AP", enter the telephone number. When you untie after entering the number, the RFC 8-RC will connect to the telephone line and redial the number with regenerated tones. You must begin dialing your number within ten seconds or the autopatch will disconnect. After you have dialed your number the autopatch timer will be set to the value programmed with the Setup Commands. This timer will reset each time you make a transmission. To shut off the autopatch enter the Autopatch Disconnect Code. The RFC 8-RC will respond with "DN" and disconnect.

REDIAL (Default) Redial *841*
Disconnect #8

To redial the last number dialed on the autopatch, enter the Autopatch Access Code followed by '*'. Enter this as one command. The RFC 8-RC will respond with "RD" and automatically dial the number. Disconnecting when the call is completed is the same as normal autopatch operation.

AUTODIAL (Default) Autodial Prefix *
Disconnect #8

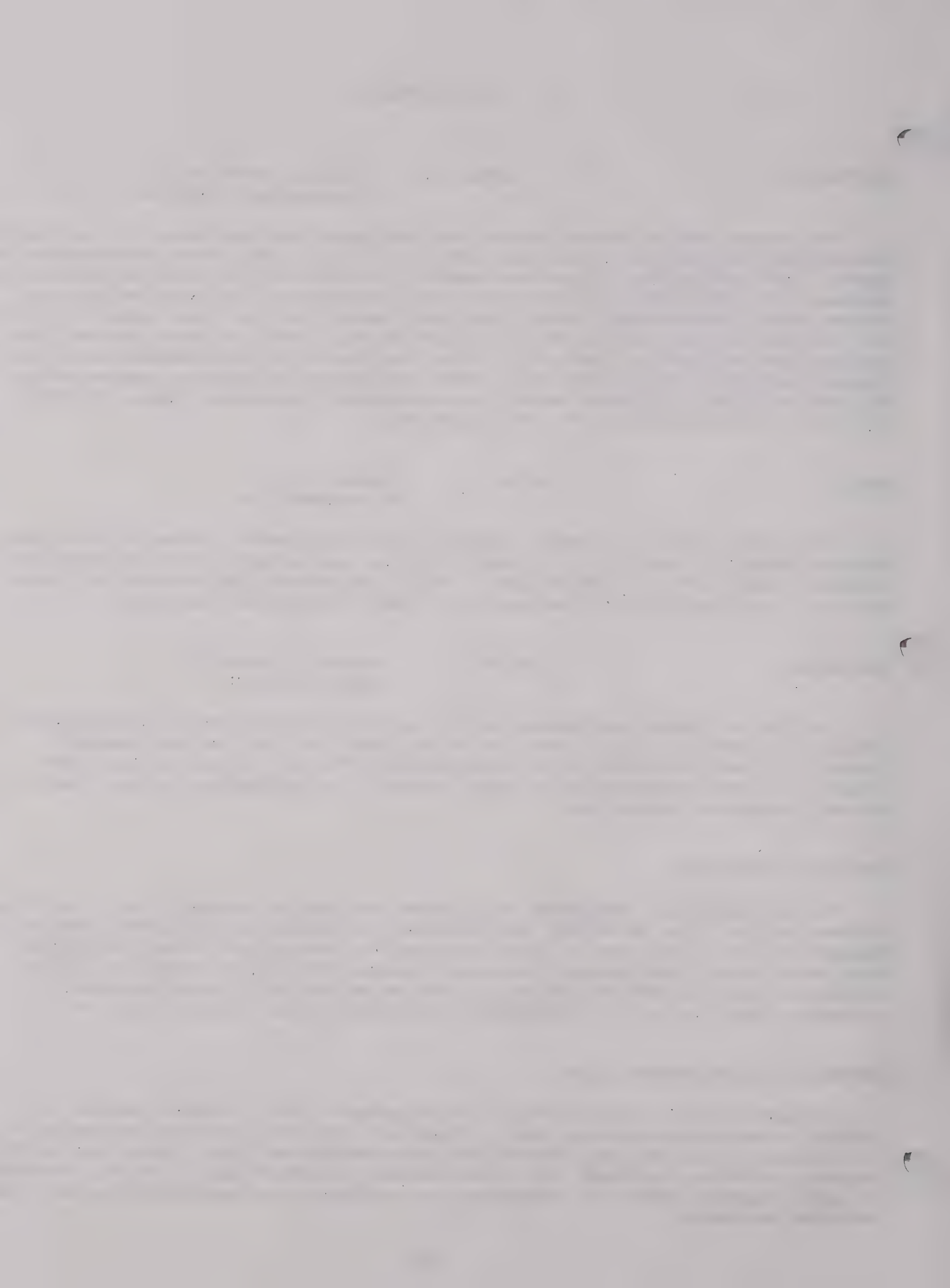
To dial a number contained in the autodial memory enter the Autodial Prefix followed by 'xx' where 'xx = 00 - 99' for the desired memory location. The controller will respond with "AD xx" and then dial your number for you. Disconnecting when the call is completed is the same as normal autopatch operation.

REVERSE AUTOPATCH

To originate an autopatch call from the the telephone line, dial the number of the line to which the RFC 8-AP is connected. The RFC 8-AP will answer the call and send a CW ID message to the caller. When the ID is complete, enter the Control Operator Access Code followed by "#". The caller on the telephone line will then be on the air. To disconnect a reverse patch, enter the Autopatch Disconnect Code followed by "#".

CONTROL VIA TELEPHONE LINE

Control of the RFC 8-RC via the telephone line is very similar to making a reverse autopatch call. After the RFC 8-RC answers and sends its ID message, commands may entered via the telephone line. Operation is the same as entering commands via radio except you MUST add a "#" to the end of each command. When all commands are completed, disconnect the same as a reverse autopatch.



LINK \ REMOTE BASE FUNCTIONS

CHANNEL SELECT (Default) 82

In the case of a multi-channel crystal link or remote base you may select one of eight channels by entering the Channel Prefix followed by the desired channel number (1-8). The RFC 8-RC will respond in CW with "CH #" where "#" is the channel number. To check which channel is currently selected, enter the Channel Select Prefix followed by '0'. The RFC 8-RC will respond with "CH #" where "#" is the channel currently selected.

FOR MORE INFORMATION SEE THE RFC 8-RC MANUAL

PIN CONNECTIONS

1 - Audio Ground	19 - Repeater Receiver COS In
2 - Repeater Receive Audio In	20 - N/C
3 - Audio +12	21 - Patch Busy
4 - N/C	22 - Ring Detect
5 - Control Receive Audio Out	23 - N/C
6 - N/C	24 - Control Receiver COS Out
7 - Repeater Receive Audio Out	25 - N/C
8 - Tone In	26 - N/C
9 - Tone Out	27 - Repeater Receiver COS Out
10 - N/C	28 - Digital Ground
11 - N/C	29 - N/C
12 - Telephone Line #1	30 - Aux Strobe
13 - N/C	31 - N/C
14 - Telephone Line #2	32 - AP Strobe
15 - N/C	33 - Aux Data 8
16 - N/C	34 - Aux Data 4
17 - Digital +12	35 - Aux Data 2
18 - N/C	36 - Aux Data 1

N/C - No Connection

WARRANTY

RF CONCEPTS, Division of Kantronics, warrants each RFC 8-AP free from defects in material and workmanship under normal use and service for a period of 1 year after the delivery to the ultimate user.

The unit must be returned to the factory, freight prepaid. The warranty card must have been submitted within 15 days after purchase. Any unauthorized repair may void this warranty.

RF CONCEPTS will provide, free of charge, both parts and labor, as necessary, to correct any defect occurring within the warranty period.

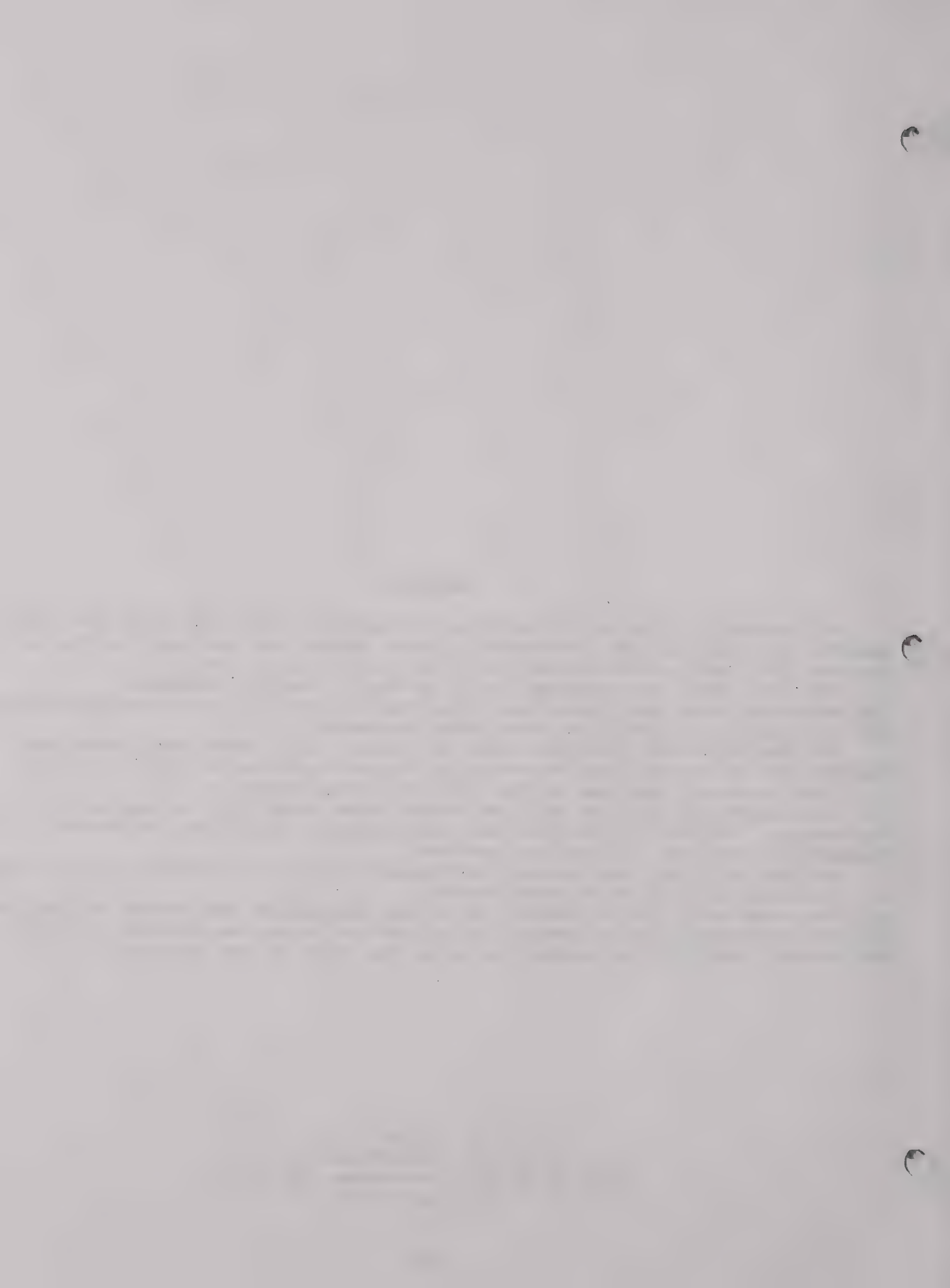
This warranty applies to the original owner only.

This warranty applies only to those units that fail during normal operation. Any unit that has been overvoltaged, modified, accidentally damaged or misused will not be covered.

RF CONCEPTS will not assume any responsibility for damage to any radio or accessory connected to this product.

This warranty is in lieu of all other warranties expressed or implied, and no representative or person is authorized to assume for RF Concepts any other liability in connection with the sale of its products.

RF CONCEPTS
Division of Kantronics
1202 E. 23 St., Lawrence, KS 66044
(913)842-7745



PIN 36

U2

74LS24

U4

74LS04

74LS00

U12

74LS04

U10

74LS04

U7

74LS00

U8

J1

U3

74LS04

74LS04

U5

74LS04

U6

74LS00

U9

J2

COMPONENT SIDE

U11

74LS04

U1

74LS00

U1

RECEIVER ☐
DTMF LEVEL ☐
TRANSMITTER ☐

PIN 1

GND
#5
#1
#6
#7
#2
#8
#3
#4

GND
#5
#1
#6
#7
#2
#8
#3
#4

AUX
OUTPUTS

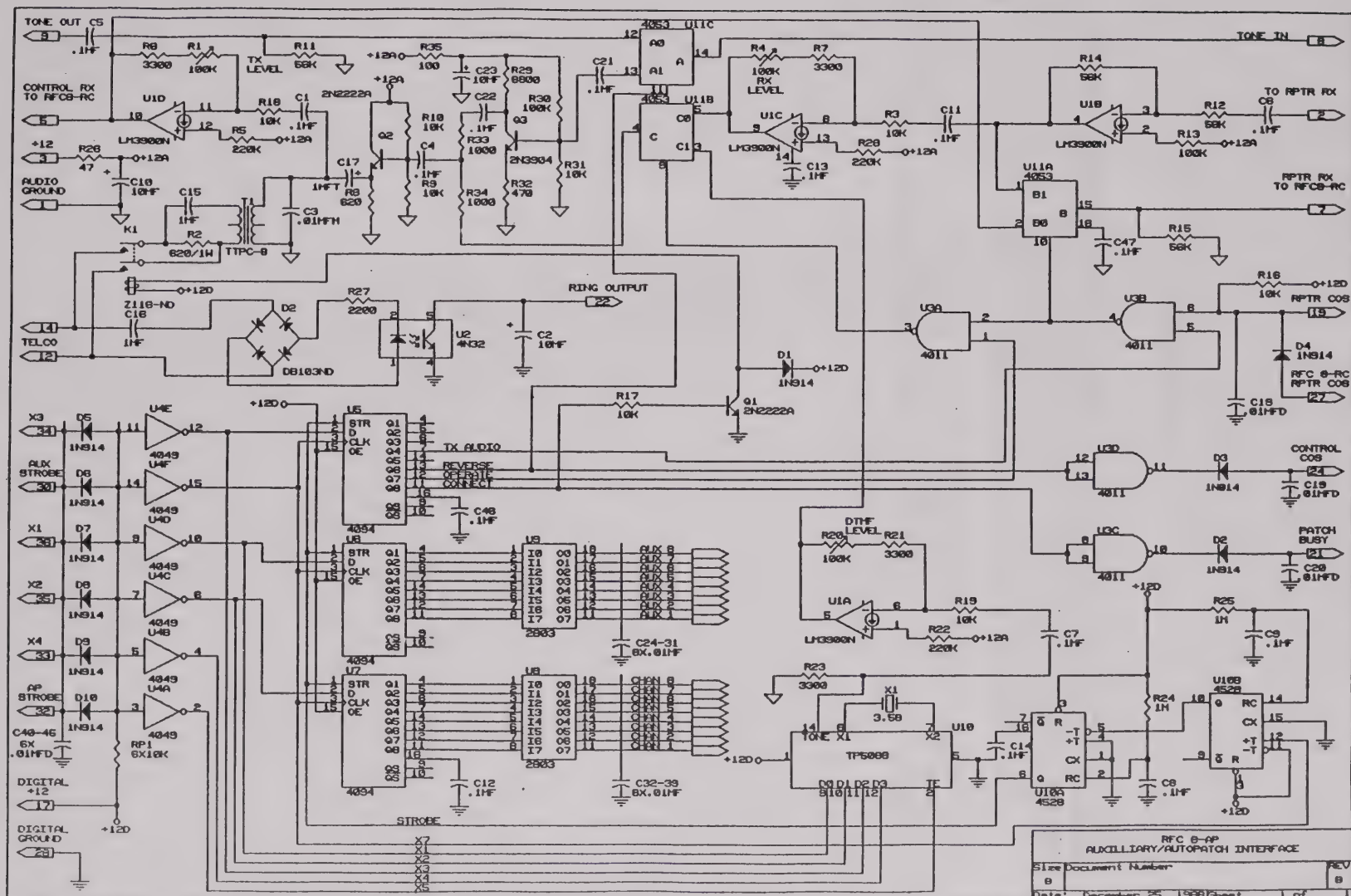
CHANNEL
SELECT
OUTPUTS

Size Document Number

A

REV

Date: November 22, 1988 Sheet of



INTRODUCTION

The RF Concepts RFC 8-RB Remote Base Interface provides the necessary control signals to interface a frequency agile transceiver to a repeater using the RFC 8-RC Repeater Controller. The RFC 8-RB has its own micro-processor which enables it to be interfaced to many different types of transceivers and also contains a remotely programmable CTCSS encoder.

The RFC 8-RB contains relays to switch the remote base signals from the remote base radio on and off the remote base bus on the RFC 8-RC. The RFC 8-RB may be programmed as remote base #1 to #8.

INSTALLATION

Installation of the RFC 8-RB is relatively simple and straight forward. There are four connections for power and ten connections to the RFC 8-RC. All connections to the remote base radio are made through the two connectors on the end of the board opposite the edge connector.

POWER SUPPLY CONNECTIONS

The RFC 8-RB requires power sources of +5 and +12 volts DC. These may be obtained from the repeater or a separate power supply. The RFC 8-RB also requires two separate ground connections. These should be connected together at the ground point and not at the edge connector. The pins for power connections are:

- Pin 1 - Audio Ground (to Pin 1 on RFC 8-RC)
- Pin 3 - Audio +12 (to +12 power source)
- Pin 17 - Digital +12 (to +12 power source)
- Pin 18 - Digital +5 (to Pin 18 on the RFC 8-RC)
- Pin 28 - Digital Ground (to Pin 28 on RFC 8-RC)

RFC 8-RC CONNECTIONS

There are ten connections to be made to the RFC 8-RC from the RFC 8-RB. These connections are made to the corresponding pins on the RFC 8-RB. These connections are:

RFC 8-RB INTERFACE	FUNCTION	RFC 8-RC CONTROLLER
Pin 2 - Remote Base Receive Audio		Pin 2
Pin 6 - Aux Transmit Audio		Pin 6
Pin 15 - Remote Base PTT		Pin 15
Pin 25 - Remote Base COS		Pin 25
Pin 29 - FREQ Strobe		Pin 29
Pin 31 - FREQ Reset		Pin 31
Pin 33 - AUX Data 8		Pin 33
Pin 34 - AUX Data 4		Pin 34
Pin 35 - AUX Data 2		Pin 35
Pin 36 - AUX Data 1		Pin 36

RADIO CONNECTIONS

The RFC 8-RB requires four connections, other than frequency control, to be made to the remote base radio. These are receive and transmit audio, receiver COS, and transmitter PTT. There is an optional CTCSS tone output on the RFC 8-RB that may be used if your system requires a remotely programmable CTCSS encoder. The level of the encoder is set by the multi-turn pot on the end of the board. All the above connections are made to the 6 pin header on the end of the board and are the same as those required of the repeater. Refer to the RFC 8-RC Owner's Manual for more information.

Pin 1 - TX Audio
Pin 2 - COS
Pin 3 - PTT
Pin 4 - RX Audio
Pin 5 - CTCSS Out
Pin 6 - Ground

FREQUENCY CONNECTIONS

The actual connections for frequency control will vary from radio to radio. Listed below are the outputs available from the RFC 8-RB. These connections are made to the 26 pin header on the end of the board.

1 MHz - Pin 22	100 KHz - Pin 23	10 KHz - Pin 15
2 MHz - Pin 24	200 KHz - Pin 21	20 KHz - Pin 13
4 MHz - Pin 26	400 KHz - Pin 19	40 KHz - Pin 11
8 MHz - Pin 25	800 KHz - Pin 17	80 KHz - Pin 9

NORMAL

+5 KHz - Pin 1
Simplex - Pin 7
Minus - Pin 5
Plus - Pin 3

INVERTED

+5 KHz - Pin 2
Simplex - Pin 8
Minus - Pin 6
Plus - Pin 4
Select - Pin 10

Frequency Common - Pin 18
Pin 20
Offset Common - Pin 12
Ground - Pin 14
Pin 16

NOTE: The Common connections are NOT ground. These pins should be tied to a supply voltage equal to that required by the PLL circuitry.

PIN CONNECTIONS

1 - Audio Ground	19 - N/C
2 - Remote Base Receiver Out	20 - N/C
3 - Audio +12	21 - N/C
4 - N/C	22 - N/C
5 - N/C	23 - N/C
6 - Aux Transmit Audio In	24 - N/C
7 - N/C	25 - Remote Base COS Out
8 - N/C	26 - N/C
9 - N/C	27 - N/C
10 - N/C	28 - Digital Ground
11 - N/C	29 - FREQ Strobe
12 - N/C	30 - N/C
13 - N/C	31 - FREQ Reset
14 - N/C	32 - N/C
15 - Remote Base PTT In	33 - AUX Data 8
16 - N/C	34 - AUX Data 4
17 - Digital +12	35 - AUX Data 2
18 - Digital +5	36 - AUX Data 1

Item	Quantity	Reference	Part	DESCRIPTION	SOURCE	PART #
1	1	U1	8085	Microprocessor	Jameco	8085A
2	1	U2	74HC573	CMOS Octal Latch	Jameco	74HC573
3	1	U3	2865A	8K EEPROM Memory	Jameco	2865A
4	2	U4,U5	4020	CMOS 16 Bit Counter	Jameco	CD4020
5	1	U6	27128	16K EPROM	Jameco	27128-25
6	1	U7	74HC138	CMOS Decoder	Jameco	74HC138
7	1	U8	8156	RAM - 1/D - TIMER	Jameco	8156
8	1	U9	4049	CMOS Buffer/Inverter	Jameco	CD4049
9	1	U10	4018	CMOS Counter	Jameco	CD4018
10	1	U11	2803	Octal Driver	Jameco	ULN2803B
11	1	U12	202	DTMF Decoder	Hall-Mark	SSI202
12	2	U13,U15	LM3900N	Operational Amplifier	Jameco	LM3900N
13	1	U14	4053	CMOS Switch	Jameco	CD4053
14	1	X1	3.2768	3.2768 MHz Crystal	Jameco	CY3.27
15	1	X2	3.58 MHZ	3.58 MHz Crystal	Jameco	CY3.57
16	2	C1,C2	22PF	22 PF Disc Capacitor	Digi-Key	P4016
17	19	C3,C6,C7,C12,C13,C14, C15,C16,C17,C18,C19,C20, C21,C26,C27,C28,C29, C30,C31	.1MF	.1 MF 50V Met. Film	Digi-Key	P4525
18	3	C4,C5,C25	10MF	10 MF 25V Tantalum	Digi-Key	P2049
19	16	C8,C9,C10,C32-47	.01MFD	.01 MF 50V Disc(.25 Spc)	Digi-Key	P4300
20	2	C11,C22	.01MFM	.01 MF Poly.	Digi-Key	P3103
21	1	C23	.001MFM	.001 MF Poly.	Digi-Key	P3102
22	1	C24	1MFB	1 MF 35V Bi-Polar	Digi-Key	P1132
23	1	R1	470	1/4 Watt 5% Resistor	Digi-Key	470Q
24	4	R2,R4,R38,R39	10K	1/4 Watt 5% Resistor	Digi-Key	10KQ
25	3	R3,R5,R28	3300	1/4 Watt 5% Resistor	Digi-Key	3.3KQ
26	13	R6,R15,R16,R18,R19,R21, R22,R24,R25,R29,R33,R34	56K	1/4 Watt 5% Resistor	Digi-Key	56KQ
27	3	R7,R8,R9	1K	1/4 Watt 5% Resistor	Digi-Key	1.0KQ
28	1	R10	1ME8	1/4 Watt 5% Resistor	Digi-Key	1.0MQ
29	2	R11,R14	36K	1/4 Watt 5% Resistor	Digi-Key	36KQ
30	4	R12,R13,R30,R36	22K	1/4 Watt 5% Resistor	Digi-Key	22KQ
31	9	R17,R20,R23,R26,R27, R32,R35,R51,R52	100K	1/4 Watt 5% Resistor	Digi-Key	100KQ
32	1	R31	39K	1/4 Watt 5% Resistor	Digi-Key	39KQ
33	1	R37	6800	1/4 Watt 5% Resistor	Digi-Key	6.8KQ
34	1	R40	620	1/4 Watt 5% Resistor	Digi-Key	620Q
35	1	R41	12K	1/4 Watt 5% Resistor	Digi-Key	12KQ
36	1	VR1	100K	100K 15 turn pot.	Digi-Key	01B15
37	2	RP1,RP2	8X10K	Resistor Pack (9)	Digi-Key	Q9103
38	3	D1,D2,D3	1N914	Switching Diode	Jameco	1N4148
39	1	Q1	2N3904	Transistor	Jameco	2N3904
40	4	Q2,Q3,Q4,Q6	2N2222A	Transistor	Jameco	2N2222A
41	1	Q5	MPF102	Field Effect Transistor	Jameco	MPF102
42	2			Crystal Insulator		
43	1			Edge Connector	Digi-Key	S1364
44	2			14 pin IC socket		
45	6			16 pin IC socket		
46	2			18 pin IC socket		
47	1			20 pin IC socket		
48	2			28 pin IC socket		
49	2			40 pin IC socket		

NOTE: Please supply resistors and diodes with either STRAIGHT leads

Item	Quantity	Reference	Part	DESCRIPTION	SOURCE	PART #
1	1	U1	8085	Microprocessor	Jameco	8085A
2	1	U2	74HC573	CMOS Octal Latch	Jameco	74HC573
3	1	U3	2865A	8K EEPROM Memory	Jameco	2865A
4	2	U4,U5	4020	CMOS 16 Bit Counter	Jameco	CD4020
5	1	U6	27128	16K EPROM	Jameco	27128-25
6	1	U7	74HC138	CMOS Decoder	Jameco	74HC138
7	1	U8	8156	RAM - 1/D - TIMER	Jameco	8156
8	1	U9	4049	CMOS Buffer/Inverter	Jameco	CD4049
9	1	U10	4018	CMOS Counter	Jameco	CD4018
10	1	U11	2803	Octal Driver	Jameco	ULN2803B
11	1	U12	202	DTMF Decoder	Hall-Mark	SSI202
12	2	U13,U15	LM3900N	Operational Amplifier	Jameco	LM3900N
13	1	U14	4053	CMOS Switch	Jameco	CD4053
14	1	X1	3.2768	3.2768 MHz Crystal	Jameco	CY3.27
15	1	X2	3.58 MHZ	3.58 MHz Crystal	Jameco	CY3.57
16	2	C1,C2	22PF	22 PF Disc Capacitor	Digi-Key	P4016
17	19	C3,C6,C7,C12,C13,C14, C15,C16,C17,C18,C19,C20, C21,C26,C27,C28,C29, C30,C31	.1MF	.1 MF 50V Met. Film	Digi-Key	P4525
18	3	C4,C5,C25	10MF	10 MF 25V Tantalum	Digi-Key	P2049
19	16	C8,C9,C10,C32-47	.01MFD	.01 MF 50V Disc(.25 Spc)	Digi-Key	P4300
20	2	C11,C22	.01MFM	.01 MF Poly.	Digi-Key	P3103
21	1	C23	.001MFM	.001 MF Poly.	Digi-Key	P3102
22	1	C24	1MFB	1 MF 35V Bi-Polar	Digi-Key	P1132
23	1	R1	470	1/4 Watt 5% Resistor	Digi-Key	470B
24	4	R2,R4,R38,R39	10K	1/4 Watt 5% Resistor	Digi-Key	10KB
25	3	R3,R5,R28	3300	1/4 Watt 5% Resistor	Digi-Key	3.3KQ
26	13	R6,R15,R16,R18,R19,R21, R22,R24,R25,R29,R33,R34	56K	1/4 Watt 5% Resistor	Digi-Key	56KQ
27	3	R7,R8,R9	1K	1/4 Watt 5% Resistor	Digi-Key	1.0KB
28	1	R10	1MEB	1/4 Watt 5% Resistor	Digi-Key	1.0MQ
29	2	R11,R14	36K	1/4 Watt 5% Resistor	Digi-Key	36KQ
30	4	R12,R13,R30,R36	22K	1/4 Watt 5% Resistor	Digi-Key	22KQ
31	9	R17,R20,R23,R26,R27, R32,R35,R51,R52	100K	1/4 Watt 5% Resistor	Digi-Key	100KQ
32	1	R31	39K	1/4 Watt 5% Resistor	Digi-Key	39KQ
33	1	R37	6800	1/4 Watt 5% Resistor	Digi-Key	6.8KQ
34	1	R40	620	1/4 Watt 5% Resistor	Digi-Key	620B
35	1	R41	12K	1/4 Watt 5% Resistor	Digi-Key	12KQ
36	1	VR1	100K	100K 15 turn pot.	Digi-Key	01B15
37	2	RP1,RP2	BX10K	Resistor Pack (9)	Digi-Key	Q9103
38	3	D1,D2,D3	1N914	Switching Diode	Jameco	1N4148
39	1	Q1	2N3904	Transistor	Jameco	2N3904
40	4	Q2,Q3,Q4,Q6	2N2222A	Transistor	Jameco	2N2222A
41	1	Q5	MPF102	Field Effect Transistor	Jameco	MPF102
42	2			Crystal Insulator		
43	1			Edge Connector	Digi-Key	S1364
44	2			14 pin IC socket		
45	6			16 pin IC socket		
46	2			18 pin IC socket		
47	1			20 pin IC socket		
48	2			28 pin IC socket		
49	2			40 pin IC socket		

NOTE: Please supply resistors and diodes with either STRAIGHT leads

Item	Quantity	Reference	Part	DESCRIPTION	SOURCE	PART #
1	1	X1	3.58 MHZ	3.58 MHz Crystal	Jameco	CY3.57
2	3	C1,C2,C8	10MF	10 MF 25V Tantalum	Digi-Key	P2049
3	4	C3,C4,C5,C6	1MF	1uf/50v Bi-Polar	Digi-Key	P1132
4	4	C7,C9,C10,C49	.1MF	.1 MF 50V Met. Film	Digi-Key	P4525
5	2	C11,C12	22PF	22 PF Disc Capacitor	Digi-Key	P4016
6	2	C13,C14	.001MFM	.001 MF Mylar	Digi-Key	P3102
7	2	C15,C16	.01MFM	.01 MF Mylar	Digi-Key	P3103
8	32	C17,C18,C19-49	.01MFD	.01 MF 50V Disc	Digi-Key	P4300
9	1	RP1	7X10K	10K/7 Element Network	Digi-Key	Q7103
10	1	RP2	9X10K	10K/9 Element Network	Digi-Key	Q9103
11	2	R1,R4	36K	1/4 Watt 5% Resistor	Digi-Key	36KQ
12	2	R2,R3	22K	1/4 Watt 5% Resistor	Digi-Key	22KQ
13	1	R5	470	1/4 Watt 5% Resistor	Digi-Key	470Q
14	2	R6,R7	10K	1/4 Watt 5% Resistor	Digi-Key	10KQ
15	4	R8,R11,R19,R20	470K	1/4 Watt Resistor	Digi-Key	470KQ
16	2	R9,R12	100K	1/4 Watt 5% Resistor	Digi-Key	100KQ
17	4	R10,R13,R14,R16	220K	1/4 Watt 5% Resistor	Digi-Key	220KQ
18	1	R15	100	1/4 Watt 5% Resistor	Digi-Key	100Q
19	1	R17	100KT	100K/15 turn Trimmer	Digi-Key	01B15
20	1	R18	3300	1/4 Watt 5% Resistor	Digi-Key	3.3KQ
21	8	D1-8	1N914	Switching Diode	Jameco	1N4148
22	1	Q1	2N2222A	Transistor	Jameco	2N2222A
23	2	K1,K2	DPDT	DPDT Relay	Same as in Amplifiers	
24	1	U1	8085	Microprocessor	Jameco	8085A
25	1	U2	74HC573	CMOS Octal Latch	Jameco	74HC573
26	3	U3A,U9A,U10A	ULN2803A	Octal Driver	Jameco	ULN2803B
27	3	U3B,U9B,U10B	UDN2981A	Octal Driver	Sprague	
28	1	U4	4018	CMOS Counter	Jameco	CD4018
29	1	U5	4049	CMOS Buffer/Inverter	Jameco	CD4049
30	1	U6	LM3900N	Operational Amplifier	Jameco	LM3900N
31	1	U7	2764	8K EPROM	Jameco	2764-45
32	1	U8	8156	RAM - I/O - TIMER	Jameco	8156
33	1	P1		26 pin Header Socket	Digi-Key	R304ND
34	1	J1		26 pin Header	Digi-Key	923863-R
35	1	P2		6 pin Header Socket	Digi-Key	WM2004
36	1	J2		6 pin Hea		

Item	Quantity	Reference	Part	DESCRIPTION	SOURCE	PART #
1	1	X1	3.58 MHZ	3.58 MHz Crystal	Jameco	CY3.57
2	3	C1,C2,C8	10MF	10 MF 25V Tantalum	Digi-Key	P2049
3	4	C3,C4,C9,C6	1MF	1uF/50v Bi-Polar	Digi-Key	P1132
4	4	C7,C9,C10,C49	.1MF	.1 MF 50V Met. Film	Digi-Key	P4525
5	2	C11,C12	22PF	22 PF Disc Capacitor	Digi-Key	P4016
6	2	C13,C14	.001MFM	.001 MF Mylar	Digi-Key	P3102
7	2	C15,C16	.01MFM	.01 MF Mylar	Digi-Key	P3103
8	32	C17,C18,C19-49	.01MFD	.01 MF 50V Disc	Digi-Key	P4300
9	1	RP1	7X10K	10K/7 Element Network	Digi-Key	Q7103
10	1	RP2	9X10K	10K/9 Element Network	Digi-Key	Q9103
11	2	R1,R4	36K	1/4 Watt 5% Resistor	Digi-Key	36KQ
12	2	R2,R3	22K	1/4 Watt 5% Resistor	Digi-Key	22KQ
13	1	R5	470	1/4 Watt 5% Resistor	Digi-Key	470Q
14	2	R6,R7	10K	1/4 Watt 5% Resistor	Digi-Key	10KQ
15	4	R8,R11,R19,R20	470K	1/4 Watt Resistor	Digi-Key	470KQ
16	2	R9,R12	100K	1/4 Watt 5% Resistor	Digi-Key	100KQ
17	4	R10,R13,R14,R16	220K	1/4 Watt 5% Resistor	Digi-Key	220KQ
18	1	R15	100	1/4 Watt 5% Resistor	Digi-Key	100Q
19	1	R17	100K7	100K/15 turn Trimmer	Digi-Key	01B15
20	1	R18	3300	1/4 Watt 5% Resistor	Digi-Key	3.3KQ
21	8	D1-B	1N914	Switching Diode	Jameco	1N4148
22	1	Q1	2N2222A	Transistor	Jameco	2N2222A
23	2	K1,K2	DPDT	DPDT Relay	Same as in Amplifiers	
24	1	U1	8085	Microprocessor	Jameco	8085A
25	1	U2	74HC573	CMOS Octal Latch	Jameco	74HC573
26	3	U3A,U9A,U10A	ULN2803A	Octal Driver	Jameco	ULN2803B
27	3	U3B,U9B,U10B	UDN2981A	Octal Driver	Sprague	
28	1	U4	4018	CMOS Counter	Jameco	CD4018
29	1	U5	4049	CMOS Buffer/Inverter	Jameco	CD4049
30	1	U6	LM3900N	Operational Amplifier	Jameco	LM3900N
31	1	U7	2764	8K EPROM	Jameco	2764-45
32	1	U8	8156	RAM - I/O - TIMER	Jameco	8156
33	1	P1		26 pin Header Socket	Digi-Key	R304ND
34	1	J1		26 pin Header	Digi-Key	923863-R
35	1	P2		6 pin Header Socket	Digi-Key	WM2004
36	1	J2		6 pin Hea		

Item	Quantity	Reference	Part	DESCRIPTION	SOURCE	PART #
1	1	U1	LM3900N	Operational Amplifier	Jameco	LM3900N
2	1	U2	4N32	Opto-Isolator	Digi-Key	4N326E
3	1	U3	4011	CMOS Quad NAND Gate	Jameco	CD4011
4	1	U4	4049	CMOS Buffer/Inverter	Jameco	CD4049
5	3	U5,U6,U7	4094	CMOS 8 Bit Register	Jameco	CD4094
6	2	U8,U9	2803	Octal Driver	Jameco	ULN2803B
7	1	U10	4528	CMOS Multi-Vibrator	Jameco	CD4528
8	1	U11	TP5088	DTMF Encoder	Jameco	TP5088
9	1	U12	4053	CMOS Analog Switch	Jameco	CD4053
10	1	K1	DPDT	12 vdc DPDT Relay	Aromat	DS2E-M
11	1	X1	3.58	3.58 MHz Crystal	Jameco	CY3.57
12	16	C1,C4,C5,C6,C7,C8,C9,C11, C12,C13,C14,C21,C22, C46,C8	.1MF	.1 MF 50V Met. Film	Digi-Key	P4525
13	3	C2,C10,C23	10MF	10 MF 25V Tantalum	Digi-Key	P2049
14	1	C3	.01MFM	.01 MF Poly.	Digi-Key	P3103
15	2	C15,C16	1MF	1uf/100v M.P. Cap.	Digi-Key	E1105
16	1	C17	1MFM	1 MF 35V Bi-Polar	Digi-Key	P1132
17	25	C18,C19,C20,C24-45	.01MFD	.01 MF 50V Disc(.25 Spc)	Digi-Key	P4300
18	3	R1,R4,R20	100K	100K 15 turn pot.	Digi-Key	01B15
19	1	R2	620/1W	1 Watt 5% Resistor	Digi-Key	620W-1
20	8	R3,R9,R10,R16,R17,R18, R19,R31	10K	1/4 Watt 5% Resistor	Digi-Key	10KQ
21	3	R5,R22,R28	220K	1/4 Watt 5% Resistor	Digi-Key	220KQ
22	4	R6,R7,R21,R23	3300	1/4 Watt 5% Resistor	Digi-Key	3.3KQ
23	1	R8	620	1/4 Watt 5% Resistor	Digi-Key	620Q
24	4	R11,R12,R14,R15	56K	1/4 Watt 5% Resistor	Digi-Key	56KQ
25	2	R13,R30	100K	1/4 Watt 5% Resistor	Digi-Key	100KQ
26	2	R24,R25	1M	1/4 Watt 5% Resistor	Digi-Key	1.0MQ
27	1	R26	47	1/4 Watt 5% Resistor	Digi-Key	47Q
28	1	R27	2200	1/4 Watt 5% Resistor	Digi-Key	2.2KQ
29	1	R29	6800	1/4 Watt 5% Resistor	Digi-Key	6.8KQ
30	1	R32	470	1/4 Watt 5% Resistor	Digi-Key	470Q
31	2	R33,R34	1000	1/4 Watt 5% Resistor	Digi-Key	1.0KQ
32	1	R35	100	1/4 Watt 5% Resistor	Digi-Key	100Q
33	1	RP1	6X10K	Resistor Pack (7)	Digi-Key	07103
34	10	D1,D3,D4,D5,D6,D7,D8,D9, D10,D11	1N914	Switching Diode	Jameco	1N4148
35	1	D2	DB103ND	Diode Bridge	Digi-Key	DB103ND
36	2	B1,Q2	2N2222A	Transistor	Jameco	2N2222A
37	1	B3	2N3904	Transistor	Jameco	2N3904
38	1	T1	TTPC-8	600/600 Transformer	Stancor	TTPC-8
39	3			14 pin IC socket		
40	6			16 pin IC socket		
41	2			18 pin IC socket		
42	1			6 pin IC socket		
43	2			9 pin jack	Digi-Key	WM4307
44	2			9 pin plug	Digi-Key	WM2007
45	20			Connector pins	Digi-Key	WM2200
46	1			Edge Connector	Digi-Key	S1364

NOTE: Please supply resistors and diodes with either STRAIGHT leads
or with leads bent to .400" centers.

Item	Quantity	Reference	Part	DESCRIPTION	SOURCE	PART #
1	1	U1	LM3900N	Operational Amplifier	Jameco	LM3900N
2	1	U2	4N32	Opto-Isolator	Digi-Key	4N326E
3	1	U3	4011	CMOS Quad NAND Gate	Jameco	CD4011
4	1	U4	4049	CMOS Buffer/Inverter	Jameco	CD4049
5	3	U5,U6,U7	4094	CMOS 8 Bit Register	Jameco	CD4094
6	2	U8,U9	2803	Octal Driver	Jameco	ULN2803B
7	1	U10	4528	CMOS Multi-Vibrator	Jameco	CD4528
8	1	U11	TP5088	DTMF Encoder	Jameco	TP5088
9	1	U12	4053	CMOS Analog Switch	Jameco	CD4053
10	1	K1	DPDT	12 vdc DPDT Relay	Aromat	DS2E-M
11	1	X1	3.58	3.58 MHz Crystal	Jameco	CY3.57
12	16	C1,C4,C5,C6,C7,C8,C9,C11, C12,C13,C14,C21,C22, C46,C8	.1MF	.1 MF 50V Met. Film	Digi-Key	P4525
13	3	C2,C10,C23	10MF	10 MF 25V Tantalum	Digi-Key	P2049
14	1	C3	.01MFH	.01 MF Poly.	Digi-Key	P3103
15	2	C15,C16	1MF	1uf/100v M.P. Cap.	Digi-Key	E1105
16	1	C17	1MFN	1 MF 35V Bi-Polar	Digi-Key	P1132
17	25	C18,C19,C20,C24-45	.01MFD	.01 MF 50V Disc(.25 Spc)	Digi-Key	P4300
18	3	R1,R4,R20	100K	100K 15 turn pot.	Digi-Key	01B15
19	1	R2	620/1W	1 Watt 5% Resistor	Digi-Key	620W-1
20	8	R3,R9,R10,R16,R17,R18, R19,R31	10K	1/4 Watt 5% Resistor	Digi-Key	10KQ
21	3	R5,R22,R28	220K	1/4 Watt 5% Resistor	Digi-Key	220KQ
22	4	R6,R7,R21,R23	3300	1/4 Watt 5% Resistor	Digi-Key	3.3KQ
23	1	R8	620	1/4 Watt 5% Resistor	Digi-Key	620Q
24	4	R11,R12,R14,R15	56K	1/4 Watt 5% Resistor	Digi-Key	56KQ
25	2	R13,R30	100K	1/4 Watt 5% Resistor	Digi-Key	100KQ
26	2	R24,R25	1M	1/4 Watt 5% Resistor	Digi-Key	1.0MQ
27	1	R26	47	1/4 Watt 5% Resistor	Digi-Key	47Q
28	1	R27	2200	1/4 Watt 5% Resistor	Digi-Key	2.2KQ
29	1	R29	6800	1/4 Watt 5% Resistor	Digi-Key	6.8KQ
30	1	R32	470	1/4 Watt 5% Resistor	Digi-Key	470Q
31	2	R33,R34	1000	1/4 Watt 5% Resistor	Digi-Key	1.0KQ
32	1	R35	100	1/4 Watt 5% Resistor	Digi-Key	100Q
33	1	RP1	6X10K	Resistor Pack (7)	Digi-Key	87103
34	10	D1,D3,D4,D5,D6,D7,D8,D9, D10,D11	1N914	Switching Diode	Jameco	1N4148
35	1	D2	DB103ND	Diode Bridge	Digi-Key	DB103ND
36	2	B1,B2	2N2222A	Transistor	Jameco	2N2222A
37	1	B3	2N3904	Transistor	Jameco	2N3904
38	1	T1	TTPC-8	600/600 Transformer	Stancor	TTPC-8
39	3			14 pin IC socket		
40	6			16 pin IC socket		
41	2			18 pin IC socket		
42	1			6 pin IC socket		
43	2			9 pin jack	Digi-Key	WM4307
44	2			9 pin plug	Digi-Key	WM2007
45	20			Connector pins	Digi-Key	WM2200
46	1			Edge Connector	Digi-Key	S1364

NOTE: Please supply resistors and diodes with either STRAIGHT leads
or with leads bent to .400" centers.

FC-BLI LINK INTERFACE

Revised: December 3, 1989

Revision: A

Bill of Materials

December 5, 1989

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Page 1

Item	Quantity	Reference	Part	DESCRIPTION	SOURCE	PART #
1	18	C1,C2,C3,C4,C11,C12,C14, C15,C17,C18,C20,C21,C23, C24,C32,C33,C34,C35	.1MF	.1 MF 50V Met. Film	Digi-Key	P4525
2	18	C5,C6,C7,C8,C13,C16,C19, C22,C25,C26	.01MFD	.01 MF 50V Disc	Digi-Key	P4300
3	3	C9,C10,C31	10MF	10 MF 25V Tantalum	Digi-Key	P2049
4	4	C27,C28,C29,C30	1MFB	1 MF 50V Bi-Polar	Digi-Key	P1132
5	6	D1,D2,D3,D4,D5,D6	1N914	Switching Diode	Jameco	1N4148
6	8	Q1,Q2,Q3,Q4,Q5,Q6,Q7,Q8	2N2222A	Transistor	Jameco	2N2222A
7	2	R1,R2	1M	1/4 Watt 5% Resistor	Digi-Key	1.0MΩ
8	2	R4,R3	100	1/4 Watt 5% Resistor	Digi-Key	100Ω
9	18	RN1,RN2,RN3,RN4,RN5, RN6,RN7,RN8,RN15,RN16	5X10K	5x10K Resistor Network	Digi-Key	Q5103
10	2	RN9,RN14	5X22K	5X22K Resistor Network	Digi-Key	Q5223
11	1	RN10	7X10K	7X10K Resistor Network	Digi-Key	Q7103
12	3	RN11,RN12,RN13	4X10K	4X10K Resistor Network	Digi-Key	Q4103
13	1	RN17	5X680	5X680 Resistor Network	Digi-Key	Q5681
14	2	U1,U12	LM3900N	Operational Amplifier	Jameco	LM3900N
15	1	U2	4049	CMOS Buffer/Inverter	Jameco	CD4049
16	8	U4,U5,U6,U7,U8,U9,U10, U11	4066	CMOS Analog Switch	Jameco	CD4066
17	1	U13	4528	CMOS Multi-Vibrator	Jameco	CD4528
18	2	U14,U15	4094	CMOS 8 Bit Register	Jameco	CD4094
19	18			14 pin IC socket		
20	4			16 pin IC socket		
21	1			36/72 pin Edge Connector		

NOTE: Please supply resistors and diodes with either STRAIGHT leads
or leads bent on .400" centers.

Item	Quantity	Reference	Part	DESCRIPTION	SOURCE	PART #
1	18	C1,C2,C3,C4,C11,C12,C14, C15,C17,C18,C20,C21,C23, C24,C32,C33,C34,C35	.1MF	.1 MF 50V Met. Film	Digi-Key	P4525
2	18	C5,C6,C7,C8,C13,C16,C19, C22,C25,C26	.01MFD	.01 MF 50V Disc	Digi-Key	P4388
3	3	C9,C10,C31	10MF	10 MF 25V Tantalum	Digi-Key	P2849
4	4	C27,C28,C29,C38	1MFB	1 MF 50V Bi-Polar	Digi-Key	P1132
5	6	D1,D2,D3,D4,D5,D6	1N914	Switching Diode	Jameco	1N4148
6	8	Q1,Q2,Q3,Q4,Q5,Q6,Q7,Q8	2N2222A	Transistor	Jameco	2N2222A
7	2	R1,R2	1M	1/4 Watt 5% Resistor	Digi-Key	1.0MΩ
8	2	R4,R3	100	1/4 Watt 5% Resistor	Digi-Key	100Ω
9	18	RN1,RN2,RN3,RN4,RN5, RN6,RN7,RN8,RN15,RN16	5X10K	5x10K Resistor Network	Digi-Key	Q5103
10	2	RN9,RN14	5X22K	5X22K Resistor Network	Digi-Key	Q5223
11	1	RN18	7X10K	7X10K Resistor Network	Digi-Key	Q7103
12	3	RN11,RN12,RN13	4X10K	4X10K Resistor Network	Digi-Key	Q4103
13	1	RN17	5X680	5X680 Resistor Network	Digi-Key	Q5681
14	2	U1,U12	LM3908N	Operational Amplifier	Jameco	LM3908N
15	1	U2	4049	CMOS Buffer/Inverter	Jameco	CD4049
16	8	U4,U5,U6,U7,U8,U9,U10, U11	4066	CMOS Analog Switch	Jameco	CD4066
17	1	U13	4528	CMOS Multi-Vibrator	Jameco	CD4528
18	2	U14,U15	4094	CMOS 8 Bit Register	Jameco	CD4094
19	18			14 pin IC socket		
20	4			16 pin IC socket		
21	1			36/72 pin Edge Connector		

NOTE: Please supply resistors and diodes with either STRAIGHT leads
or leads bent on .400" centers.

RFC 8-RC Repeater Controller Board

The RFC 8-RC Repeater Controller provides you with all the flexibility and expandability you'll need for your repeater. The single board controller provides for complete operation of your standard repeater, including your control link and remote base transceiver.

Four COS inputs provide for prioritized selection of the input signal, allowing local users to override link signals. With the optional RFC 8-RB Remote Base interface, you can have up to 8 remote base stations connected to your system, providing the ability to build complete network systems with just a few components.

The RFC 8-RC also has on-board CTCSS circuitry to eliminate interference from adjacent repeaters on the same frequency, or to provide limited access to the controllers programming. The RFC 8-RC has built in EEPROM memory for storing your favorite settings, eliminating the need for battery backup systems. The built-in watchdog timer samples the controller processor clock, and resets the controller should the processor lock up for any reason.

The optional Autopatch controller (RFC 8-AP) provides complete telephone autopatch interface, with programmable speed-dial numbers you can assign to your club members, emergency phone numbers, or even long distance access codes.

Security codes provide for three access levels, allowing you to provide limited access to the functions of the controller.

All programming is accomplished through the TouchTone™ pad on your standard transceiver, over the air, so you no longer need to take a computer to the site (or even make a trip to the site) to change the system operation. (Some programming requires a 16-key TouchTone™ pad.)

All of this on a 4.5 x 6.5 inch PC board which requires only 5VDC at 300 ma. And if this isn't enough, you get a full one-year warranty on parts and labor.

Suggested Retail \$395.00

Features

- 4 COS Inputs
- 3 PTT Outputs
- 0.4 to 4 seconds Hang Delay Timer
- 0.5 to 3.0 minutes Timeout Timer
- 10 to 30 wpm CW Speed
- 400 to 3000 Hz Tone Frequencies
- Remotely Programmable
- Data stored in non-volatile EEPROM
- 8-bit Expansion Port
- 1 Link Control
(up to 8 with optional RFC 8-AP)
- 1 Remote Base Control
(up to 8 with optional RFC 8-RB)
- 8085A Microprocessor
- Power: 5 VDC at 300 ma
- 4.5 inches x 6.5 inches
- Card Edge Connector
(36/72 pin x .100 spacing)
- 1 year Warranty (parts and labor)

Options

- RFC 8-AP Autopatch
- RFC 8-RB Remote Base Interface



Contact your favorite dealer

Inquiries

2000 Humboldt St., Reno, NV 89509
(702) 827-0133

Factory

1202 E. 23rd Street, Lawrence, KS 66046
(913) 842-7745

rfconcepts is a Division of Kantronics, Inc.

Dear Sir,

I have the pleasure to acknowledge the receipt of your letter of the 14th inst. in relation to the above matter.

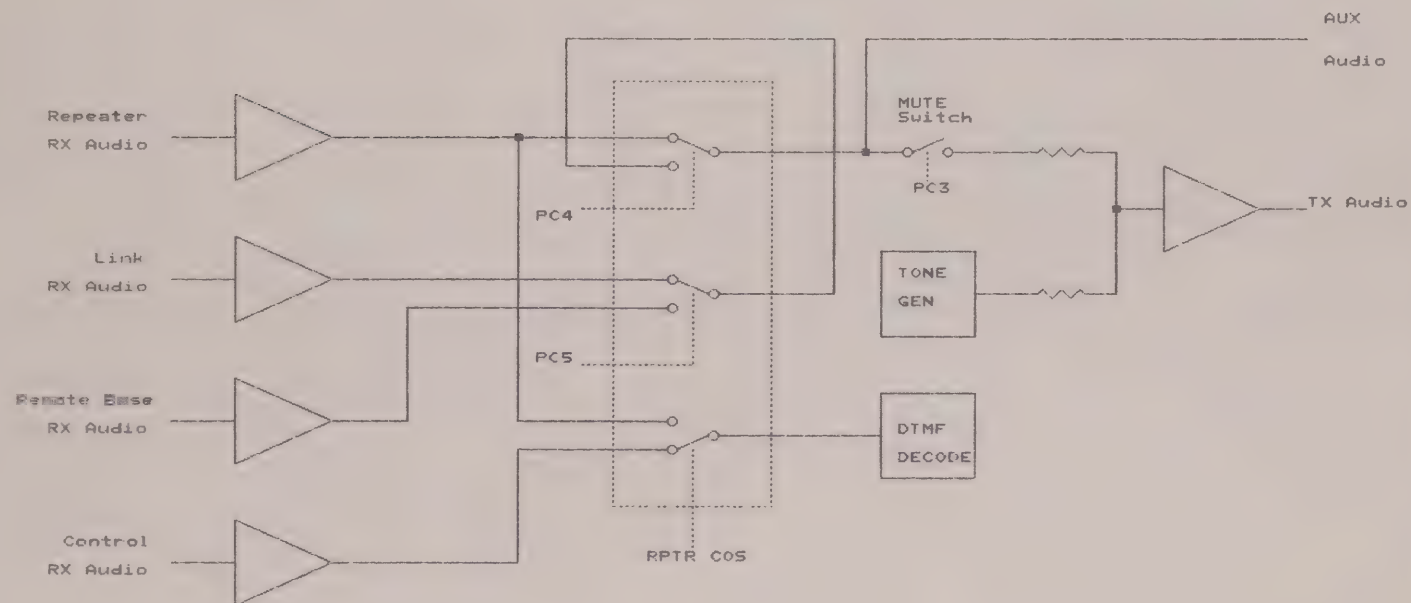
The information provided in your letter has been forwarded to the relevant authorities for their consideration.

I am sure that you will be satisfied with the outcome of the process.

Yours faithfully,

[Signature]

[Name]



RC-8 Simplified Audio Diagram

Size Document Number

REV

Date: February 17, 1991 Sheet

of

RC-8 Port/Memory Assignments

MEMORY			
0000 - 3FFF	EPROM	27128	16K X 8
4000 - 5FFF	EEPROM	2865A	8K X 8
8000 - 80FF	RAM	8156	256 X 8

IO	
40	DTMF DECODE SSI 202
80	PIA Command/Status
81	PIA Port A
82	PIA Port B
83	PIA Port C
84	PIA Timer Low 8 Bits
85	PIA Timer Hi 6 Bits and Mode

PIA Command

7	6	5	4	3	2	1	0
TM ₂	TM ₁	IEB	IEA	PC ₂	PC ₁	PB	PA

PA: 1 = Output; 0 = Input

PB: 1 = Output; 0 = Input

PIA Status

7	6	5	4	3	2	1	0
X	TIMR	INT B	B BF	IRQ B	INT A	A BF	IRQ A

Port A (OUTPUT)

7	6	5	4	3	2	1	0
FREQ STB	AUX STB	FREQ RESET	AP STB	X8	X4	X2	X1

Port B (INPUT)

7	6	5	4	3	2	1	0
ALARM	BUSY	RING	CTCSS	CTL COS	RMT COS	LINK COS	RPTR COS

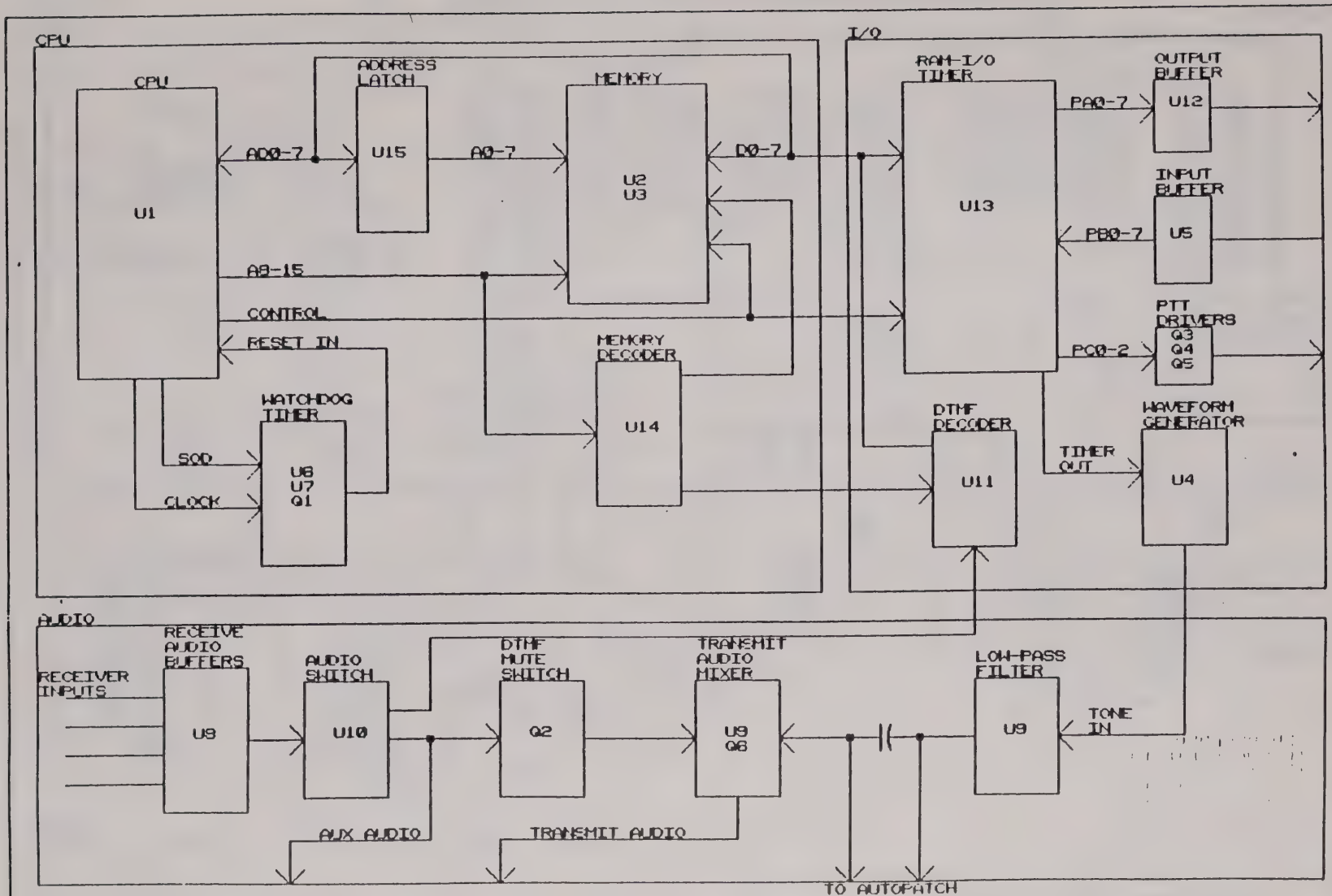
Port C (INPUT)

7	6	5	4	3	2	1	0
X	X	AUD 2 SWT	AUD 1 SWT	AUD MUTE	RMT PTT	LINK PTT	RPTR PTT

AUD 1 SWT: 0 =
AUD 2 SWT: 0 =

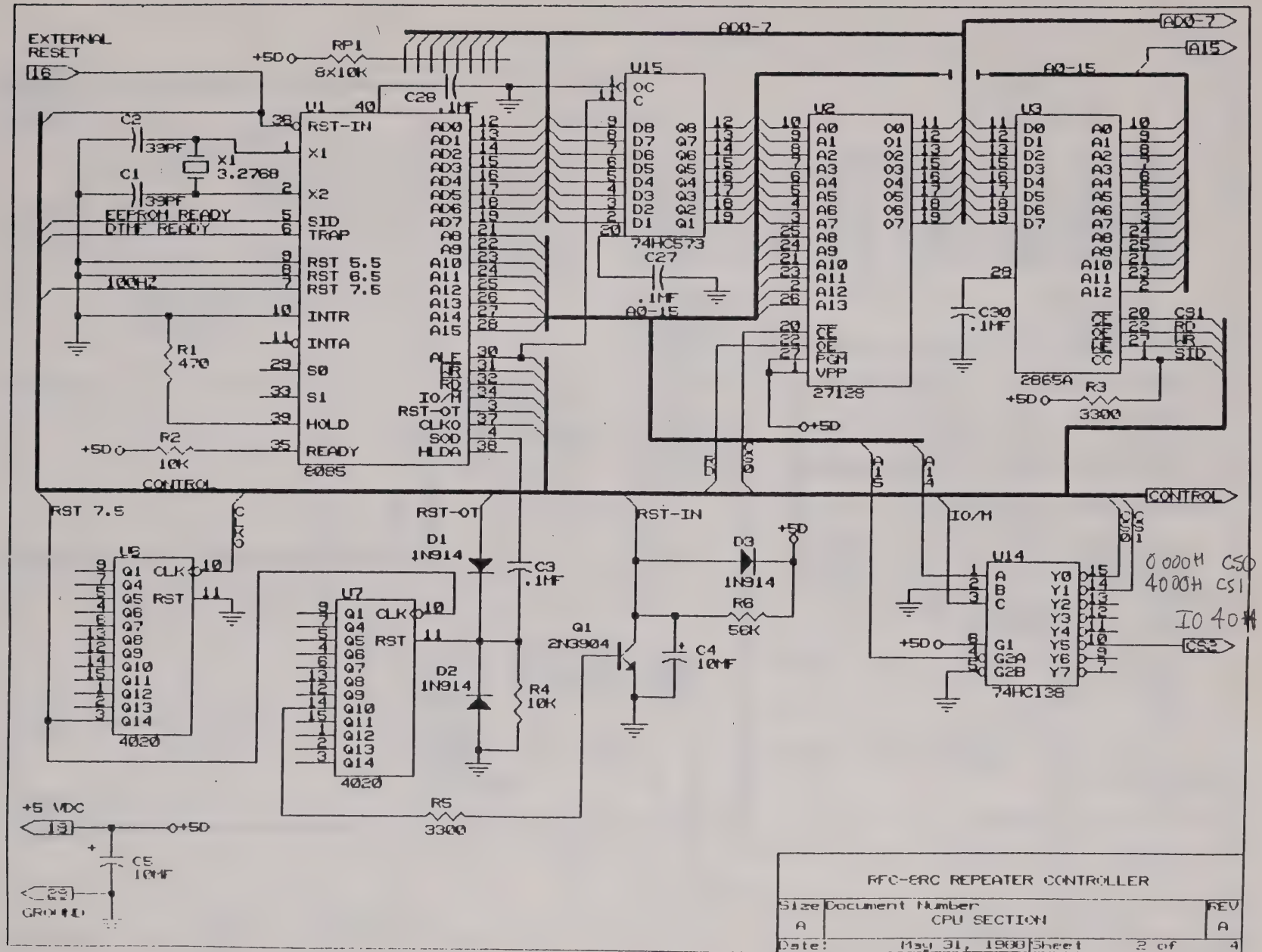
; 1 =
; 1 =

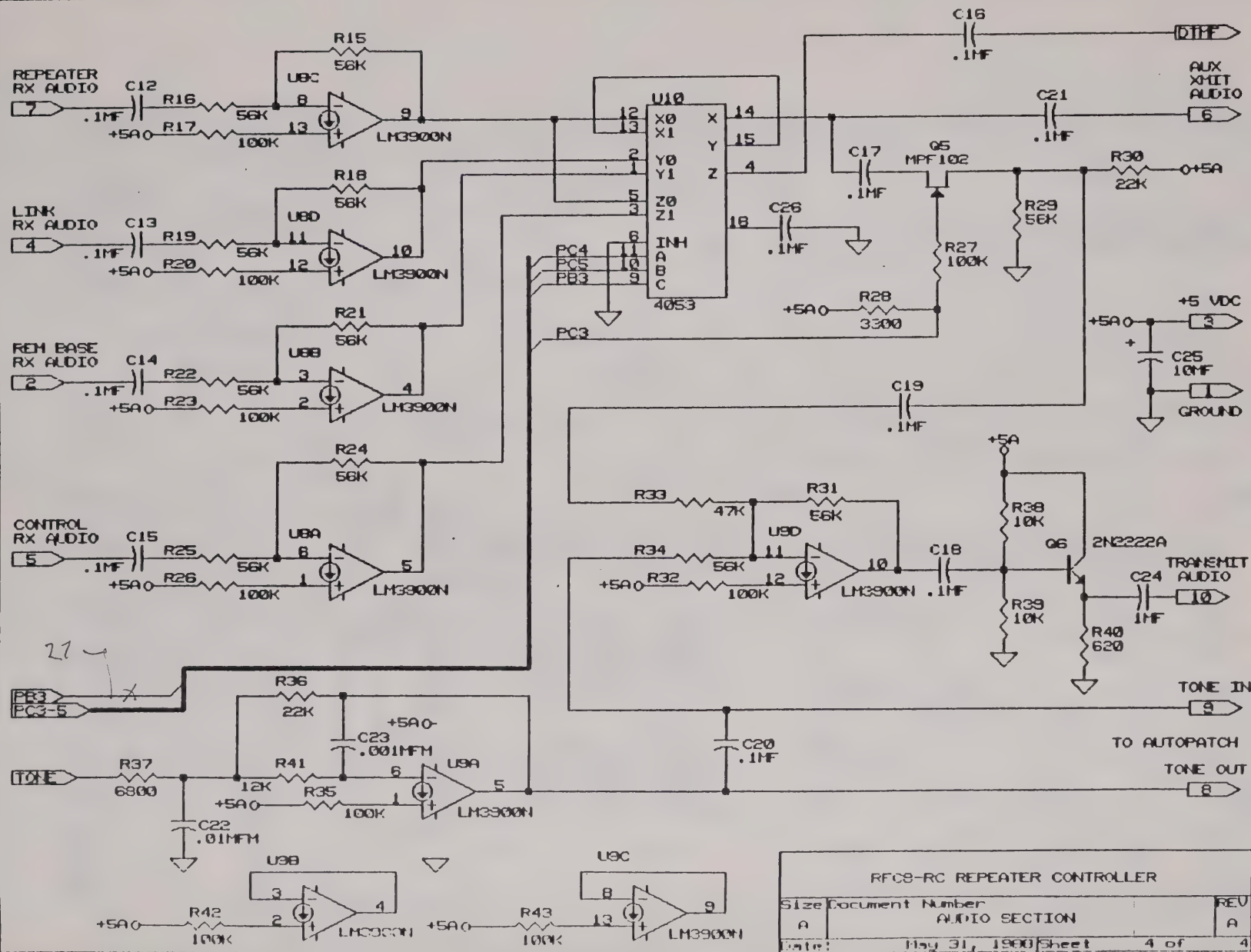
0 = RPTR
0 = LINK } 1 = LINK OR RB
1 = RB }



RFC9-RC REPEATER CONTROLLER

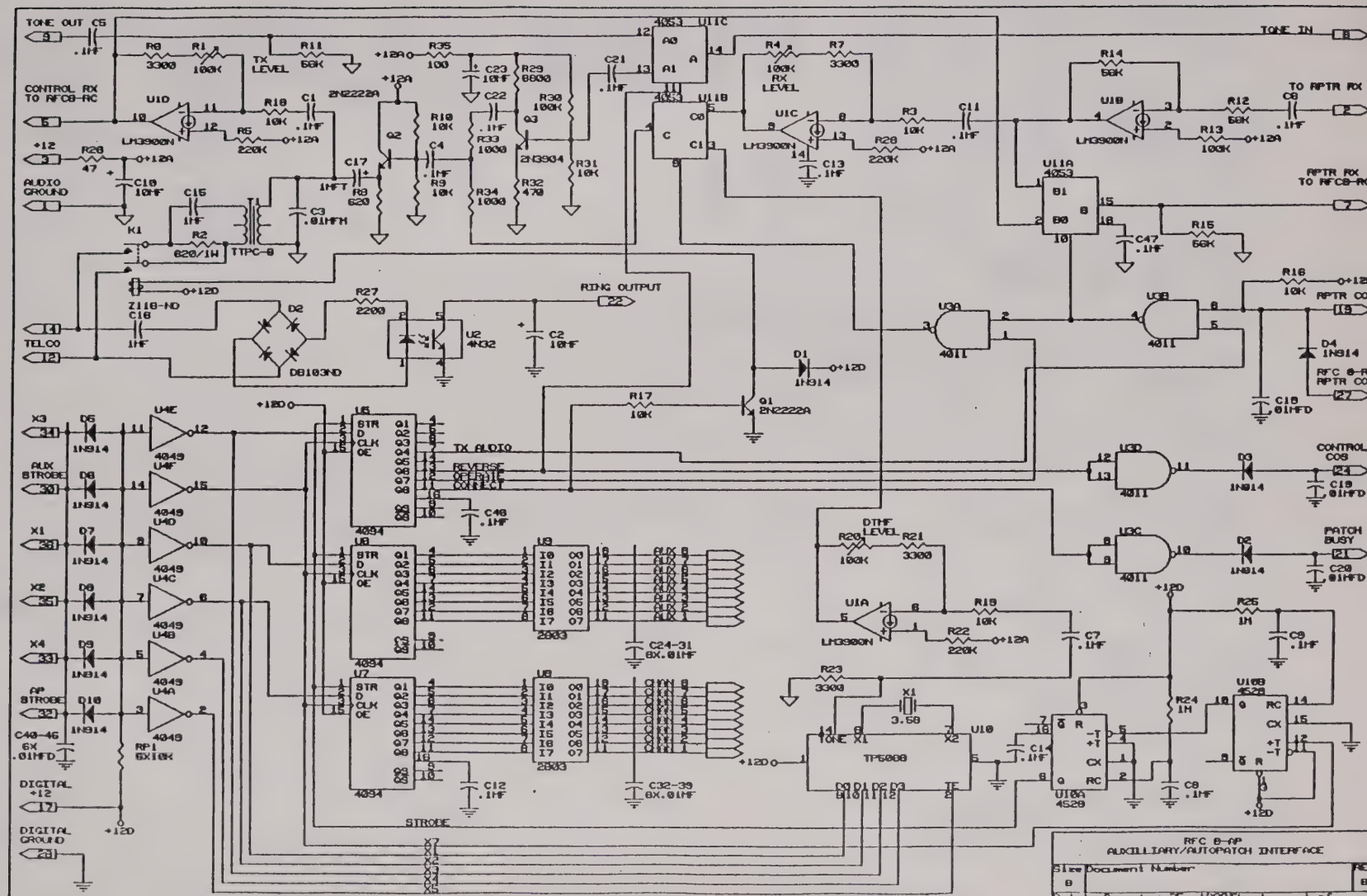
Size	Document Number	REV
A	BLOCK/FLOW DIAGRAM	A
Date:	May 31, 1988	Sheet 1 of 4

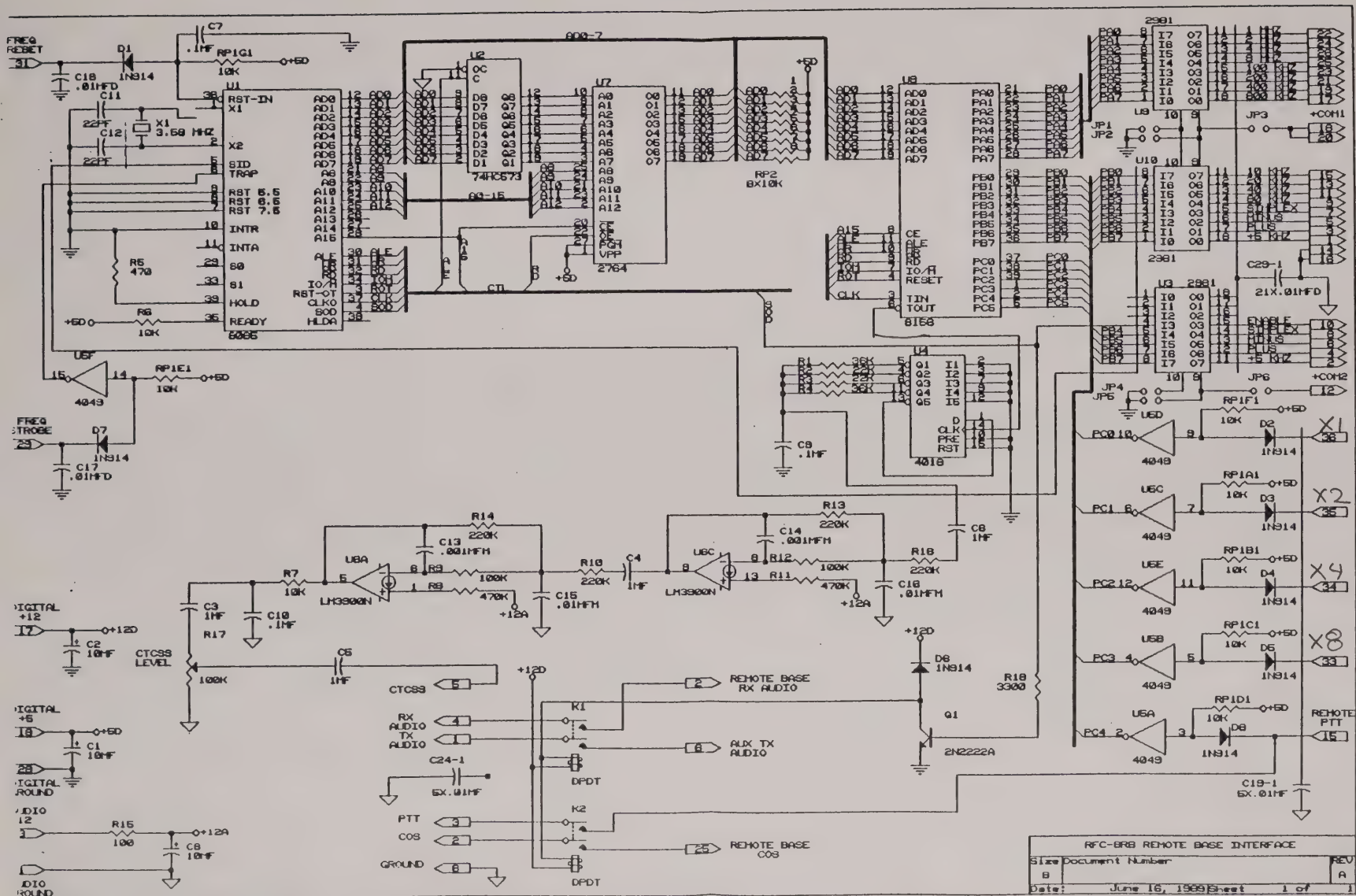




RFCS-RC REPEATER CONTROLLER

Size	Document Number	REV
A	AUDIO SECTION	A
Date:	May 31, 1980	Sheet 4 of 4







8085AH/8085AH-2/8085AH-1 8-BIT HMOS MICROPROCESSORS

- Single +5V Power Supply with 10% Voltage Margins
- 3 MHz, 5 MHz and 6 MHz Selections Available
- 20% Lower Power Consumption than 8085A for 3 MHz and 5 MHz
- 1.3 μ s Instruction Cycle (8085AH); 0.8 μ s (8085AH-2); 0.67 μ s (8085AH-1)
- 100% Compatible with 8085A
- 100% Software Compatible with 8080A
- On-Chip Clock Generator (with External Crystal, LC or RC Network)
- On-Chip System Controller; Advanced Cycle Status Information Available for Large System Control
- Four Vectored Interrupt Inputs (One is Non-Maskable) Plus an 8080A-Compatible Interrupt
- Serial In/Serial Out Port
- Decimal, Binary and Double Precision Arithmetic
- Direct Addressing Capability to 64K Bytes of Memory
- Available in EXPRESS
 - Standard Temperature Range
 - Extended Temperature Range

The Intel® 8085AH is a complete 8 bit parallel Central Processing Unit (CPU) implemented in N-channel, depletion load, silicon gate technology (HMOS). Its instruction set is 100% software compatible with the 8080A microprocessor, and it is designed to improve the present 8080A's performance by higher system speed. Its high level of system integration allows a minimum system of three IC's [8085AH (CPU), 8156H (RAM/IO) and 8755A (EPROM/IO)] while maintaining total system expandability. The 8085AH-2 and 8085AH-1 are faster versions of the 8085 AH.

The 8085AH incorporates all of the features that the 8224 (clock generator) and 8228 (system controller) provided for the 8080A, thereby offering a high level of system integration.

The 8085AH uses a multiplexed data bus. The address is split between the 8 bit address bus and the 8 bit data bus. The on-chip address latches of 8155H/8156H/8755A memory products allow a direct interface with the 8085AH.

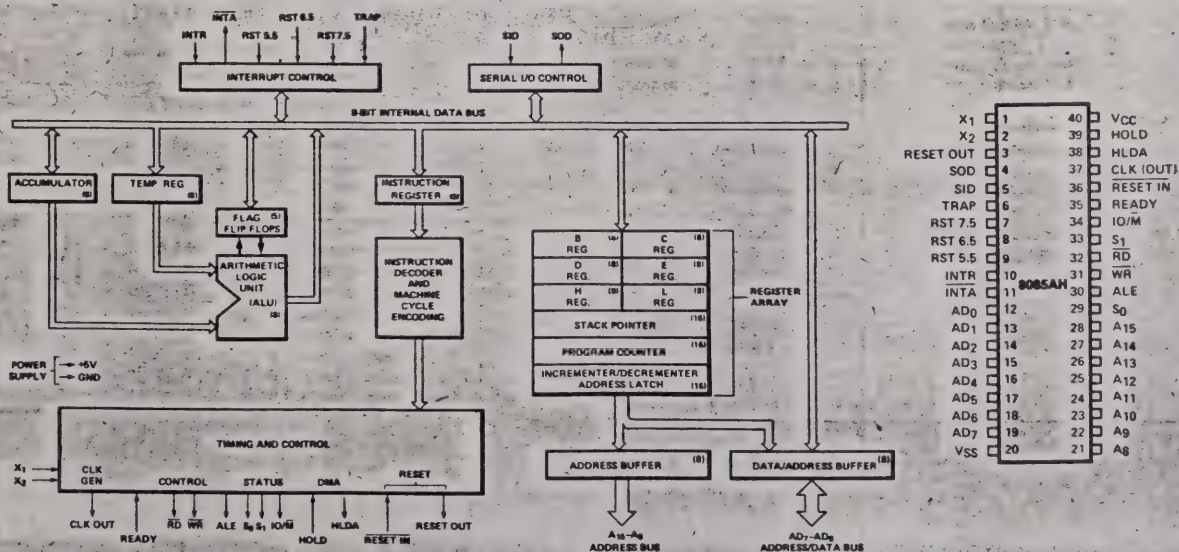


Figure 1. 8085AH CPU Functional Block Diagram

Figure 2. 8085AH Pin Configuration

Table 1. Pin Description

Symbol	Type	Name and Function																																												
A ₈ -A ₁₅	O	Address Bus: The most significant 8 bits of the memory address or the 8 bits of the I/O address, 3-stated during Hold and Halt modes and during RESET.																																												
AD ₀ -7	I/O	Multiplexed Address/Data Bus: Lower 8 bits of the memory address (or I/O address) appear on the bus during the first clock cycle (T state) of a machine cycle. It then becomes the data bus during the second and third clock cycles.																																												
ALE	O	Address Latch Enable: It occurs during the first clock state of a machine cycle and enables the address to get latched into the on-chip latch of peripherals. The falling edge of ALE is set to guarantee setup and hold times for the address information. The falling edge of ALE can also be used to strobe the status information. ALE is never 3-stated.																																												
S ₀ , S ₁ , and IO/M	O	Machine Cycle Status: <table><tr><th>IO/M</th><th>S₁</th><th>S₀</th><th>Status</th></tr><tr><td>0</td><td>0</td><td>1</td><td>Memory write</td></tr><tr><td>0</td><td>1</td><td>0</td><td>Memory read</td></tr><tr><td>1</td><td>0</td><td>1</td><td>I/O write</td></tr><tr><td>1</td><td>1</td><td>0</td><td>I/O read</td></tr><tr><td>0</td><td>1</td><td>1</td><td>Opcode fetch</td></tr><tr><td>1</td><td>1</td><td>1</td><td>Opcode fetch</td></tr><tr><td>1</td><td>1</td><td>1</td><td>Interrupt Acknowledge</td></tr><tr><td>•</td><td>0</td><td>0</td><td>Halt</td></tr><tr><td>•</td><td>X</td><td>X</td><td>Hold</td></tr><tr><td>•</td><td>X</td><td>X</td><td>Reset</td></tr></table> <p>• = 3-state (high impedance) X = unspecified</p> <p>S₁ can be used as an advanced R/W status. IO/M, S₀ and S₁ become valid at the beginning of a machine cycle and remain stable throughout the cycle. The falling edge of ALE may be used to latch the state of these lines.</p>	IO/M	S ₁	S ₀	Status	0	0	1	Memory write	0	1	0	Memory read	1	0	1	I/O write	1	1	0	I/O read	0	1	1	Opcode fetch	1	1	1	Opcode fetch	1	1	1	Interrupt Acknowledge	•	0	0	Halt	•	X	X	Hold	•	X	X	Reset
IO/M	S ₁	S ₀	Status																																											
0	0	1	Memory write																																											
0	1	0	Memory read																																											
1	0	1	I/O write																																											
1	1	0	I/O read																																											
0	1	1	Opcode fetch																																											
1	1	1	Opcode fetch																																											
1	1	1	Interrupt Acknowledge																																											
•	0	0	Halt																																											
•	X	X	Hold																																											
•	X	X	Reset																																											
RD	O	Read Control: A low level on RD indicates the selected memory or I/O device is to be read and that the Data Bus is available for the data transfer, 3-stated during Hold and Halt modes and during RESET.																																												
WR	O	Write Control: A low level on WR indicates the data on the Data Bus is to be written into the selected memory or I/O location. Data is set up at the trailing edge of WR. 3-stated during Hold and Halt modes and during RESET.																																												

Symbol	Type	Name and Function
READY	I	Ready: If READY is high during a read or write cycle, it indicates that the memory or peripheral is ready to send or receive data. If READY is low, the cpu will wait an integral number of clock cycles for READY to go high before completing the read or write cycle. READY must conform to specified setup and hold times.
HOLD	I	Hold: Indicates that another master is requesting the use of the address and data buses. The cpu, upon receiving the hold request, will relinquish the use of the bus as soon as the completion of the current bus transfer. Internal processing can continue. The processor can regain the bus only after the HOLD is removed. When the HOLD is acknowledged, the Address, Data RD, WR, and IO/M lines are 3-stated.
HLDA	O	Hold Acknowledge: Indicates that the cpu has received the HOLD request and that it will relinquish the bus in the next clock cycle. HLDA goes low after the Hold request is removed. The cpu takes the bus one half clock cycle after HLDA goes low.
INTR	I	Interrupt Request: Is used as a general purpose interrupt. It is sampled only during the next to the last clock cycle of an instruction and during Hold and Halt states. If it is active, the Program Counter (PC) will be inhibited from incrementing and an INTA will be issued. During this cycle a RESTART or CALL instruction can be inserted to jump to the interrupt service routine. The INTR is enabled and disabled by software. It is disabled by Reset and immediately after an interrupt is accepted.
INTA	O	Interrupt Acknowledge: Is used instead of (and has the same timing as) RD during the instruction cycle after an INTR is accepted. It can be used to activate an 8259A Interrupt chip or some other Interrupt port.
RST 5.5 RST 6.5 RST 7.5	I	<p>Restart Interrupts: These three inputs have the same timing as INTR except they cause an internal RESTART to be automatically inserted.</p> <p>The priority of these interrupts is ordered as shown in Table 2. These interrupts have a higher priority than INTR. In addition, they may be individually masked out using the SIM instruction.</p>

Table 1. Pin Description (Continued)

Symbol	Type	Name and Function	Symbol	Type	Name and Function
TRAP	I	Trap: Trap interrupt is a non-maskable RESTART interrupt. It is recognized at the same time as INTR or RST 5.5-7.5. It is unaffected by any mask or Interrupt Enable. It has the highest priority of any interrupt. (See Table 2.)	RESET OUT	O	Reset Out: Reset Out indicates cpu is being reset. Can be used as a system reset. The signal is synchronized to the processor clock and lasts an integral number of clock periods.
RESET IN	I	Reset In: Sets the Program Counter to zero and resets the Interrupt Enable and HLDA flip-flops. The data and address buses and the control lines are 3-stated during RESET and because of the asynchronous nature of RESET, the processor's internal registers and flags may be altered by RESET with unpredictable results. RESET IN is a Schmitt-triggered input, allowing connection to an R-C network for power-on RESET delay (see Figure 3). Upon power-up, RESET IN must remain low for at least 10 ms after minimum VCC has been reached. For proper reset operation after the power-up duration, RESET IN should be kept low a minimum of three clock periods. The CPU is held in the reset condition as long as RESET IN is applied.	X ₁ , X ₂	I	X₁ and X₂: Are connected to a crystal, LC, or RC network to drive the internal clock generator. X ₁ can also be an external clock input from a logic gate. The input frequency is divided by 2 to give the processor's internal operating frequency.
			CLK	O	Clock: Clock output for use as a system clock. The period of CLK is twice the X ₁ , X ₂ input period.
			SID	I	Serial Input Data Line: The data on this line is loaded into accumulator bit 7 whenever a RIM instruction is executed.
			SOD	O	Serial Output Data Line: The output SOD is set or reset as specified by the SIM instruction.
			VCC		Power: +5 volt supply.
			VSS		Ground: Reference.

Table 2. Interrupt Priority, Restart Address, and Sensitivity

Name	Priority	Address Branched To (1) When Interrupt Occurs	Type Trigger
TRAP	1	24H	Rising edge AND high level until sampled.
RST 7.5	2	3CH	Rising edge (latched).
RST 6.5	3	34H	High level until sampled.
RST 5.5	4	2CH	High level until sampled.
INTR	5	See Note (2).	High level until sampled.

NOTES:

1. The processor pushes the PC on the stack before branching to the indicated address.
2. The address branched to depends on the instruction provided to the cpu when the interrupt is acknowledged.

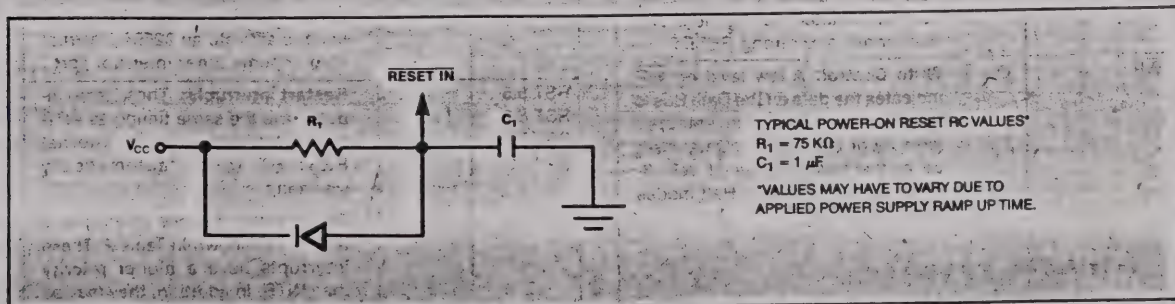


Figure 3. Power-On Reset Circuit

FUNCTIONAL DESCRIPTION

The 8085AH is a complete 8-bit parallel central processor. It is designed with N-channel, depletion load, silicon gate technology (HMOS), and requires a single +5 volt supply. Its basic clock speed is 3 MHz (8085AH), 5 MHz (8085AH-2), or 6 MHz (8085AH-1), thus improving on the present 8080A's performance with higher system speed. Also it is designed to fit into a minimum system of three IC's: The CPU (8085AH), a RAM/IO (8156H), and an EPROM/IO chip (8755A).

The 8085AH has twelve addressable 8-bit registers. Four of them can function only as two 16-bit register pairs. Six others can be used interchangeably as 8-bit registers or as 16-bit register pairs. The 8085AH register set is as follows:

Mnemonic	Register	Contents
ACC or A	Accumulator	8 bits
PC	Program Counter	16-bit address
BC,DE,HL	General-Purpose Registers; data pointer (HL)	8 bits x 6 or 16 bits x 3
SP	Stack Pointer	16-bit address
Flags or F	Flag Register	5 flags (8-bit space)

The 8085AH uses a multiplexed Data Bus. The address is split between the higher 8-bit Address Bus and the lower 8-bit Address/Data Bus. During the first T state (clock cycle) of a machine cycle the low order address is sent out on the Address/Data bus. These lower 8 bits may be latched externally by the Address Latch Enable signal (ALE). During the rest of the machine cycle the data bus is used for memory or I/O data.

The 8085AH provides \overline{RD} , \overline{WR} , S_0 , S_1 , and IO/\overline{M} signals for bus control. An Interrupt Acknowledge signal (\overline{INTA}) is also provided. \overline{HOLD} and all interrupts are synchronized with the processor's internal clock. The 8085AH also provides Serial Input Data (SID) and Serial Output Data (SOD) lines for simple serial interface.

In addition to these features, the 8085AH has three maskable, vector interrupt pins, one nonmaskable TRAP interrupt, and a bus vectored interrupt, INTR.

INTERRUPT AND SERIAL I/O

The 8085AH has 5 interrupt inputs: INTR, RST 5.5, RST 6.5, RST 7.5, and TRAP. INTR is identical in function to the 8080A INT. Each of the three RESTART inputs, 5.5, 6.5, and 7.5, has a programmable mask. TRAP is also a RESTART interrupt but it is nonmaskable.

The three maskable interrupts cause the internal execution of RESTART (saving the program counter in the stack and branching to the RESTART address) if the interrupts are enabled and if the interrupt mask is not set. The nonmaskable TRAP causes the internal execution of a RESTART vector independent of the state of the interrupt enable or masks. (See Table 2.)

There are two different types of inputs in the restart interrupts. RST 5.5 and RST 6.5 are *high level-sensitive* like INTR (and INT on the 8080) and are recognized with the same timing as INTR. RST 7.5 is *rising edge-sensitive*.

For RST 7.5, only a pulse is required to set an internal flip-flop which generates the internal interrupt request (a normally high level signal with a low going pulse is recommended for highest system noise immunity). The RST 7.5 request flip-flop remains set until the request is serviced. Then it is reset automatically. This flip-flop may also be reset by using the SIM instruction or by issuing a RESET IN to the 8085AH. The RST 7.5 internal flip-flop will be set by a pulse on the RST 7.5 pin even when the RST 7.5 interrupt is masked out.

The status of the three RST interrupt masks can only be affected by the SIM instruction and RESET IN. (See SIM, Chapter 5 of the MCS-80/85 User's Manual.)

The interrupts are arranged in a fixed priority that determines which interrupt is to be recognized if more than one is pending as follows: TRAP—highest priority, RST 7.5, RST 6.5, RST 5.5, INTR—lowest priority. This priority scheme does not take into account the priority of a routine that was started by a higher priority interrupt. RST 5.5 can interrupt an RST 7.5 routine if the interrupts are re-enabled before the end of the RST 7.5 routine.

The TRAP interrupt is useful for catastrophic events such as power failure or bus error. The TRAP input is recognized just as any other interrupt but has the highest priority. It is not affected by any flag or mask. The TRAP input is both *edge and level sensitive*. The TRAP input must go high and remain high until it is acknowledged. It will not be recognized again until it goes low, then high again. This avoids any false triggering due to noise or logic glitches. Figure 4 illustrates the TRAP interrupt request circuitry within the 8085AH. Note that the servicing of any interrupt (TRAP, RST 7.5, RST 6.5, RST 5.5, INTR) disables all future interrupts (except TRAPs) until an EI instruction is executed.

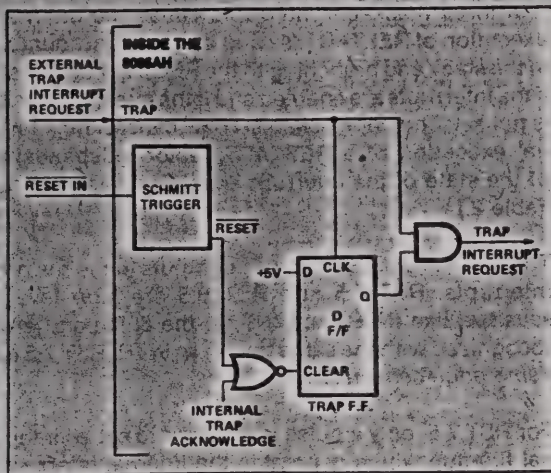


Figure 4. TRAP and RESET IN Circuit

The TRAP interrupt is special in that it disables interrupts, but preserves the previous interrupt enable status. Performing the first RIM instruction following a TRAP interrupt allows you to determine whether interrupts were enabled or disabled prior to the TRAP. All subsequent RIM instructions provide current interrupt enable status. Performing a RIM instruction following INTR, or RST 5.5-7.5 will provide current Interrupt Enable status, revealing that interrupts are disabled. See the description of the RIM instruction in the MCS-80/85 Family User's Manual.

The serial I/O system is also controlled by the RIM and SIM instructions. SID is read by RIM, and SIM sets the SOD data.

DRIVING THE X₁ AND X₂ INPUTS

You may drive the clock inputs of the 8085AH, 8085AH-2, or 8085AH-1 with a crystal, an LC tuned circuit, an RC network, or an external clock source. The crystal frequency must be at least 1 MHz, and must be twice the desired internal clock frequency; hence, the 8085AH is operated with a 6 MHz crystal (for 3 MHz clock), the 8085AH-2 operated with a 10 MHz crystal (for 5 MHz clock), and the 8085AH-1 can be operated with a 12 MHz crystal (for 6 MHz clock). If a crystal is used, it must have the following characteristics:

Parallel resonance at twice the clock frequency desired

C_L (load capacitance) ≤ 30 pF

C_S (shunt capacitance) ≤ 7 pF

R_S (equivalent shunt resistance) ≤ 75 Ohms

Drive level: 10 mW

Frequency tolerance: $\pm .005\%$ (suggested)

Note the use of the 20 pF capacitor between X₂ and ground. This capacitor is required with crystal frequencies below 4 MHz to assure oscillator startup at the correct frequency. A parallel-resonant LC circuit may be used as the frequency-determining network for the 8085AH, providing that its frequency tolerance of approximately $\pm 10\%$ is acceptable. The components are chosen from the formula:

$$f = \frac{1}{2\pi\sqrt{L(C_{ext} + C_{int})}}$$

To minimize variations in frequency, it is recommended that you choose a value for C_{ext} that is at least twice that of C_{int} , or 30 pF. The use of an LC circuit is not recommended for frequencies higher than approximately 5 MHz.

An RC circuit may be used as the frequency-determining network for the 8085AH if maintaining a precise clock frequency is of no importance. Variations in the on-chip timing generation can cause a wide variation in frequency when using the RC mode. Its advantage is its low component cost. The driving frequency generated by the circuit shown is approximately 3 MHz. It is not recommended that frequencies greatly higher or lower than this be attempted.

Figure 5 shows the recommended clock driver circuits. Note in D and E that pullup resistors are required to assure that the high level voltage of the input is at least 4V and maximum low level voltage of 0.8V.

For driving frequencies up to and including 6 MHz you may supply the driving signal to X₁ and leave X₂ open-circuited (Figure 5D). If the driving frequency is from 6 MHz to 12 MHz, stability of the clock generator will be improved by driving both X₁ and X₂ with a push-pull source (Figure 5E). To prevent self-oscillation of the 8085AH, be sure that X₂ is not coupled back to X₁ through the driving circuit.

Table 6. Instruction Set Summary

Mnemonic	Instruction Code D ₇ D ₆ D ₅ D ₄ D ₃ D ₂ D ₁ D ₀	Operations Description
MOVE, LOAD, AND STORE		
MOV r1 r2	0 1 D D D S S S	Move register to register
MOV M.r	0 1 1 1 0 S S S	Move register to memory
MOV r.M	0 1 D D D 1 1 0	Move memory to register
MVI r	0 0 D D D 1 J 0	Move immediate register
MVI M	0 0 1 1 0 1 1 0	Move immediate memory
LXI B	0 0 0 0 0 0 0 1	Load immediate register Pair B & C
LXI D	0 0 0 1 0 0 0 1	Load immediate register Pair D & E
LXI H	0 0 1 0 0 0 0 1	Load immediate register Pair H & L
STAX B	0 0 0 0 0 0 1 0	Store A indirect
STAX D	0 0 0 1 0 0 1 0	Store A indirect
LDAX B	0 0 0 0 1 0 1 0	Load A indirect
LDAX D	0 0 0 1 1 0 1 0	Load A indirect
STA	0 0 1 1 0 0 1 0	Store A direct
LDA	0 0 1 1 1 0 1 0	Load A direct
SHLD	0 0 1 0 0 0 1 0	Store H & L direct
LHLD	0 0 1 0 1 0 1 0	Load H & L direct
XCHG	1 1 1 0 1 0 1 1	Exchange D & E, H & L Registers
STACK OPS		
PUSH B	1 1 0 0 0 1 0 1	Push register Pair B & C on stack
PUSH D	1 1 0 1 0 1 0 1	Push register Pair D & E on stack
PUSH H	1 1 1 0 0 1 0 1	Push register Pair H & L on stack
PUSH PSW	1 1 1 1 0 1 0 1	Push A and Flags on stack
POP B	1 1 0 0 0 0 0 1	Pop register Pair B & C off stack
POP D	1 1 0 1 0 0 0 1	Pop register Pair D & E off stack
POP H	1 1 1 0 0 0 0 1	Pop register Pair H & L off stack
POP PSW	1 1 1 1 0 0 0 1	Pop A and Flags off stack
XTHL	1 1 1 0 0 0 1 1	Exchange top of stack, H & L
SPHL	1 1 1 1 1 0 0 1	H & L to stack pointer
LXI SP	0 0 1 1 0 0 0 1	Load immediate stack pointer
INX SP	0 0 1 1 0 0 1 1	Increment stack pointer
DCX SP	0 0 1 1 1 0 1 1	Decrement stack pointer
JUMP		
JMP	1 1 0 0 0 0 1 1	Jump unconditional
JC	1 1 0 1 1 0 1 0	Jump on carry
JNC	1 1 0 1 0 0 1 0	Jump on no carry
JZ	1 1 0 0 1 0 1 0	Jump on zero
JNZ	1 1 0 0 0 0 1 0	Jump on no zero
JP	1 1 1 1 0 0 1 0	Jump on positive
JM	1 1 1 1 1 0 1 0	Jump on minus
JPE	1 1 1 0 1 0 1 0	Jump on parity even
JPO	1 1 1 0 0 0 1 0	Jump on parity odd
PCHL	1 1 1 0 1 0 0 1	H & L to program counter
CALL		
CALL	1 1 0 0 1 1 0 1	Call unconditional
CC	1 1 0 1 1 1 0 0	Call on carry
CNC	1 1 0 1 0 1 0 0	Call on no carry

Mnemonic	Instruction Code D ₇ D ₆ D ₅ D ₄ D ₃ D ₂ D ₁ D ₀	Operations Description
CZ	1 1 0 0 0 1 1 0 0	Call on zero
CNZ	1 1 0 0 0 0 1 0 0	Call on no zero
CP	1 1 1 1 0 0 1 0 0	Call on positive
CM	1 1 1 1 1 0 0 0	Call on minus
CPE	1 1 1 0 1 1 0 0	Call on parity even
CPO	1 1 1 0 0 1 0 0	Call on parity odd
RETURN		
RET	1 1 0 0 0 1 0 0 1	Return
RC	1 1 0 0 1 1 0 0 0	Return on carry
RNC	1 1 0 0 1 0 0 0 0	Return on no carry
RZ	1 1 0 0 0 1 0 0 0	Return on zero
RNZ	1 1 0 0 0 0 0 0 0	Return on no zero
RP	1 1 1 1 0 0 0 0 0	Return on positive
RM	1 1 1 1 1 0 0 0 0	Return on minus
RPE	1 1 1 0 1 0 0 0 0	Return on parity even
RPO	1 1 1 0 0 0 0 0 0	Return on parity odd
RESTART		
RST	1 1 A A A 1 1 1	Restart
INPUT/OUTPUT		
IN	1 1 0 1 1 0 1 1 1	Input
OUT	1 1 0 1 0 0 1 1 1	Output
INCREMENT AND DECREMENT		
INR r	0 0 D D D 1 0 0	Increment register
DCR r	0 0 D D D 1 0 1	Decrement register
INR M	0 0 1 1 0 1 0 0	Increment memory
DCR M	0 0 1 1 0 1 0 1	Decrement memory
INX B	0 0 0 0 0 0 1 1	Increment B & C registers
INX D	0 0 0 1 0 0 1 1	Increment D & E registers
INX H	0 0 1 0 0 0 1 1	Increment H & L registers
DCX B	0 0 0 0 1 0 1 1	Decrement B & C
DCX D	0 0 0 1 1 0 1 1	Decrement D & E
DCX H	0 0 1 0 1 0 1 1	Decrement H & L
ADD		
ADD r	1 0 0 0 0 S S S	Add register to A
ADC r	1 0 0 0 1 S S S	Add register to A with carry
ADD M	1 0 C 0 0 1 1 0	Add memory to A
ADC M	1 0 0 0 1 1 1 0	Add memory to A with carry
ADI	1 1 0 0 0 1 1 0	Add immediate to A
ACI	1 1 0 0 1 1 1 0	Add immediate to A with carry
DAD B	0 0 0 0 1 0 0 1	Add B & C to H & L
DAD D	0 0 0 1 1 0 0 1	Add D & E to H & L
DAD H	0 0 1 0 1 0 0 1	Add H & L to H & L
DAD SP	0 0 1 1 1 0 0 1	Add stack pointer to H & L
SUBTRACT		
SUB r	1 0 0 1 0 S S S	Subtract register from A
SBB r	1 0 0 1 1 S S S	Subtract register from A with borrow
SUB M	1 0 0 1 0 1 1 0	Subtract memory from A
SBB M	1 0 0 1 1 1 1 0	Subtract memory from A with borrow
SUI	1 1 0 1 0 1 1 0	Subtract immediate from A
SBI	1 1 0 1 1 1 1 0	Subtract immediate from A with borrow

Table 6. Instruction Set Summary (Continued)

Mnemonic	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀	Operations Description
LOGICAL									
ANA r	1	0	1	0	0	S	S	S	And register with A
XRA r	1	0	1	0	1	S	S	S	Exclusive OR register with A
ORA r	1	0	1	1	0	S	S	S	OR register with A
CMP r	1	0	1	1	1	S	S	S	Compare register with A
ANA M	1	0	1	0	0	1	1	0	And memory with A
XRA M	1	0	1	0	1	1	1	0	Exclusive OR memory with A
ORA M	1	0	1	1	0	1	1	0	OR memory with A
CMP M	1	0	1	1	1	1	1	0	Compare memory with A
ANI	1	1	1	0	0	1	1	0	And immediate with A
XRI	1	1	1	0	1	1	1	0	Exclusive OR immediate with A
ORI	1	1	1	1	0	1	1	0	OR immediate with A
CPI	1	1	1	1	1	1	1	0	Compare immediate with A
ROTATE									
RLC	0	0	0	0	0	1	1	1	Rotate A left
RRC	0	0	0	0	1	1	1	1	Rotate A right
RAL	0	0	0	1	0	1	1	1	Rotate A left through carry
RAR	0	0	0	1	1	1	1	1	Rotate A right through carry

NOTES:

1. DDS or SSS: B 000, C 001, D 010, E 011, H 100, L 101, Memory 110, A 111.
2. Two possible cycle times (6/12) indicate instruction cycles dependent on condition flags.

*All mnemonics copyrighted ©Intel Corporation 1976.

Mnemonic	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀	Operations Description
SPECIALS									
CMA	0	0	1	0	1	1	1	1	Complement A
STC	0	0	1	1	0	1	1	1	Set carry
CMC	0	0	1	1	1	1	1	1	Complement carry
DAA	0	0	1	0	0	1	1	1	Decimal adjust A
CONTROL									
EI	1	1	1	1	1	0	1	1	Enable interrupts
DI	1	1	1	1	0	0	1	1	Disable interrupt
NOP	0	0	0	0	0	0	0	0	No-operation
HLT	0	1	1	1	0	1	1	0	Halt
NEW 8085AH INSTRUCTIONS									
RIM	0	0	1	0	0	0	0	0	Read Interrupt Mask
SIM	0	0	1	1	0	0	0	0	Set Interrupt Mask

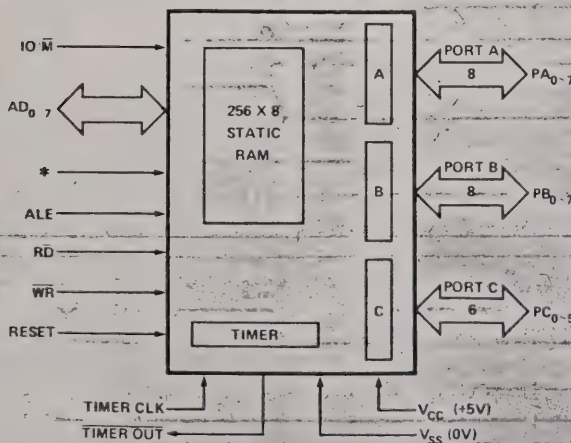
8155H/8156H/8155H-2/8156H-2 2048-BIT STATIC HMOS RAM WITH I/O PORTS AND TIMER

- Single +5V Power Supply with 10% Voltage Margins
- 30% Lower Power Consumption than the 8155 and 8156
- 100% Compatible with 8155 and 8156
- 256 Word x 8 Bits
- Completely Static Operation
- Internal Address Latch
- 2 Programmable 8-Bit I/O Ports
- 1 Programmable 6-Bit I/O Port
- Programmable 14-Bit Binary Counter/Timer
- Compatible with 8085AH, 8085A and 8088 CPU
- Multiplexed Address and Data Bus
- Available in EXPRESS
 - Standard Temperature Range
 - Extended Temperature Range

The Intel® 8155H and 8156H are RAM and I/O chips implemented in N-Channel, depletion load, silicon gate technology (HMOS), to be used in the 8085AH and 8088 microprocessor systems. The RAM portion is designed with 2048 static cells organized as 256 x 8. They have a maximum access time of 400 ns to permit use with no wait states in 8085AH CPU. The 8155H-2 and 8156H-2 have maximum access times of 330 ns for use with the 8085AH-2 and the 5 MHz 8088 CPU.

The I/O portion consists of three general purpose I/O ports. One of the three ports can be programmed to be status pins, thus allowing the other two ports to operate in handshake mode.

A 14-bit programmable counter/timer is also included on chip to provide either a square wave or terminal count pulse for the CPU system depending on timer mode.



* 8155H/8155H-2 = \overline{CE} , 8156H/8156H-2 = CE

Figure 1. Block Diagram

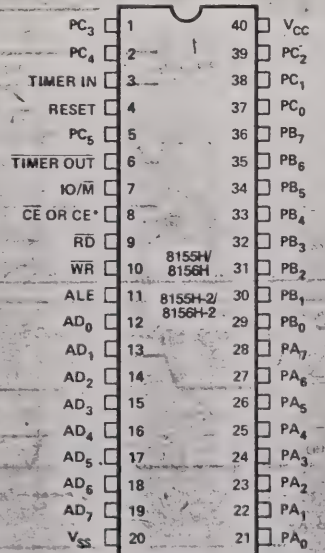


Figure 2. Pin Configuration

Table 1. Pin Description

Symbol	Type	Name and Function
RESET	I	Reset: Pulse provided by the 8085AH to initialize the system (connect to 8085AH RESET OUT). Input high on this line resets the chip and initializes the three I/O ports to input mode. The width of RESET pulse should typically be two 8085AH clock cycle times.
AD ₀₋₇	I/O	Address/Data: 3-state Address/Data lines that interface with the CPU lower 8-bit Address/Data Bus. The 8-bit address is latched into the address latch inside the 8155H/56H on the falling edge of ALE. The address can be either for the memory section or the I/O section depending on the IO/M input. The 8-bit data is either written into the chip or read from the chip, depending on the \overline{WR} or \overline{RD} input signal.
CE or \overline{CE}	I	Chip Enable: On the 8155H, this pin is \overline{CE} and is ACTIVE LOW. On the 8156H, this pin is CE and is ACTIVE HIGH.
\overline{RD}	I	Read Control: Input low on this line with the Chip Enable active enables and AD ₀₋₇ buffers. If IO/M pin is low, the RAM content will be read out to the AD bus. Otherwise the content of the selected I/O port or command/status registers will be read to the AD bus.
\overline{WR}	I	Write Control: Input low on this line with the Chip Enable active causes the data on the Address/Data bus to be written to the RAM or I/O ports and command/status register, depending on IO/M.
ALE	I	Address Latch Enable: This control signal latches both the address on the AD ₀₋₇ lines and the state of the Chip Enable and IO/M into the chip at the falling edge of ALE.
IO/M	I	I/O Memory: Selects memory if low and I/O and command/status registers if high.
PA ₀₋₇ (8)	I/O	Port A: These 8 pins are general purpose I/O pins. The in/out direction is selected by programming the command register.
PB ₀₋₇ (8)	I/O	Port B: These 8 pins are general purpose I/O pins. The in/out direction is selected by programming the command register.
PC ₀₋₅ (6)	I/O	Port C: These 6 pins can function as either input port, output port, or as control signals for PA and PB. Programming is done through the command register. When PC ₀₋₅ are used as control signals, they will provide the following: PC ₀ — A INTR (Port A Interrupt) PC ₁ — ABF (Port A Buffer Full) PC ₂ — A STB (Port A Strobe) PC ₃ — B INTR (Port B Interrupt) PC ₄ — B BF (Port B Buffer Full) PC ₅ — B STB (Port B Strobe)
TIMER IN	I	Timer Input: Input to the counter-timer.
TIMER OUT	O	Timer Output: This output can be either a square wave or a pulse, depending on the timer mode.
V _{CC}		Voltage: +5 volt supply.
V _{SS}		Ground: Ground reference.

FUNCTIONAL DESCRIPTION

The 8155H/8156H contains the following:

- 2k Bit Static RAM organized as 256 x 8
- Two 8-bit I/O ports (PA & PB) and one 6-bit I/O port (PC)
- 14-bit timer-counter

The IO/M (IO/Memory Select) pin selects either the five registers (Command, Status, PA₀₋₇, PB₀₋₇, PC₀₋₅) or the memory (RAM) portion.

The 8-bit address on the Address/Data lines, Chip Enable input CE or \overline{CE} , and IO/M are all latched on-chip at the falling edge of ALE.

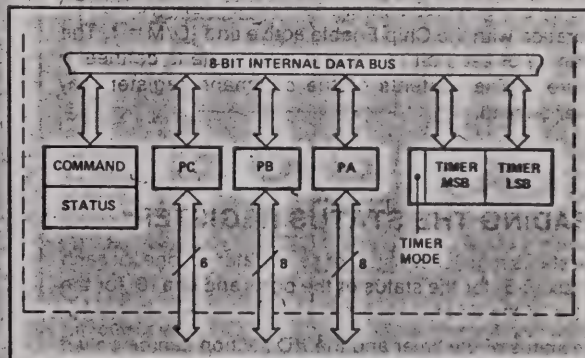


Figure 3. 8155H/8156H Internal Registers

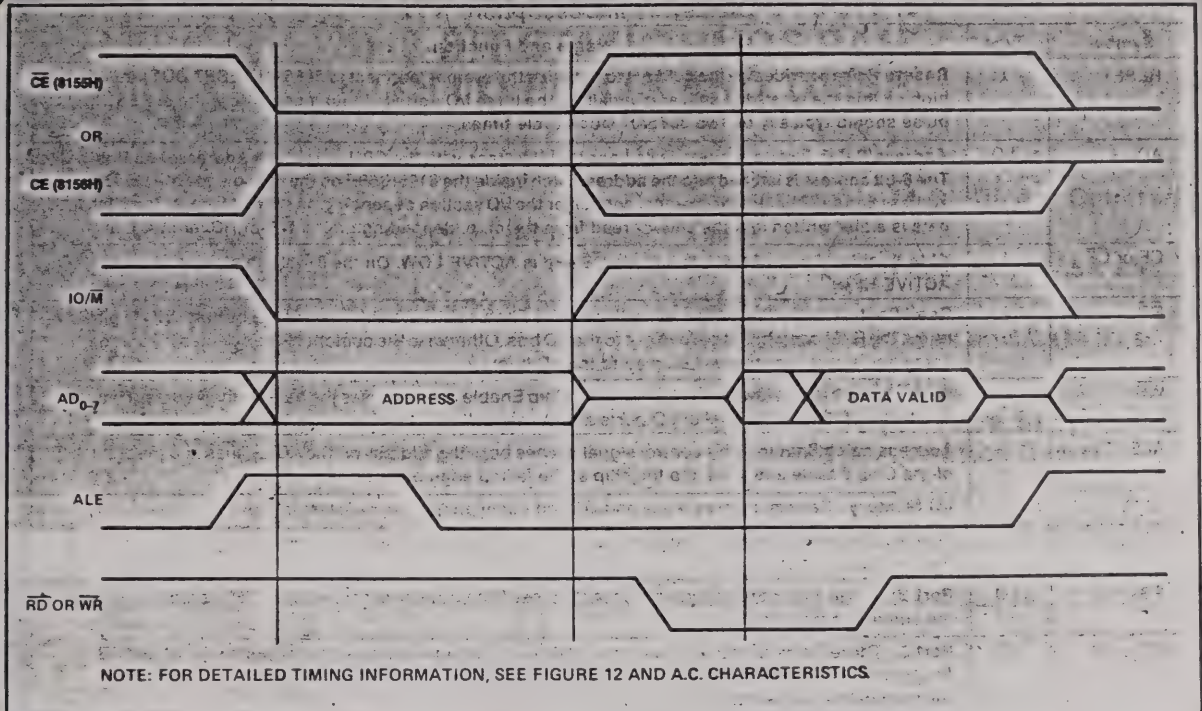


Figure 4. 8155H/8156H On-Board Memory Read/Write Cycle

PROGRAMMING OF THE COMMAND REGISTER

The command register consists of eight latches. Four bits (0-3) define the mode of the ports, two bits (4-5) enable or disable the interrupt from port C when it acts as control port, and the last two bits (6-7) are for the timer.

The command register contents can be altered at any time by using the I/O address XXXX000 during a WRITE operation with the Chip Enable active and $\text{IO}/\overline{\text{M}} = 1$. The meaning of each bit of the command byte is defined in Figure 5. The contents of the command register may never be read.

READING THE STATUS REGISTER

The status register consists of seven latches, one for each bit; six (0-5) for the status of the ports and one (6) for the status of the timer.

The status of the timer and the I/O section can be polled by reading the Status Register (Address XXXX000). Status word format is shown in Figure 6. Note that you may never write to the status register since the command register shares the same I/O address and the command register is selected when a write to that address is issued.

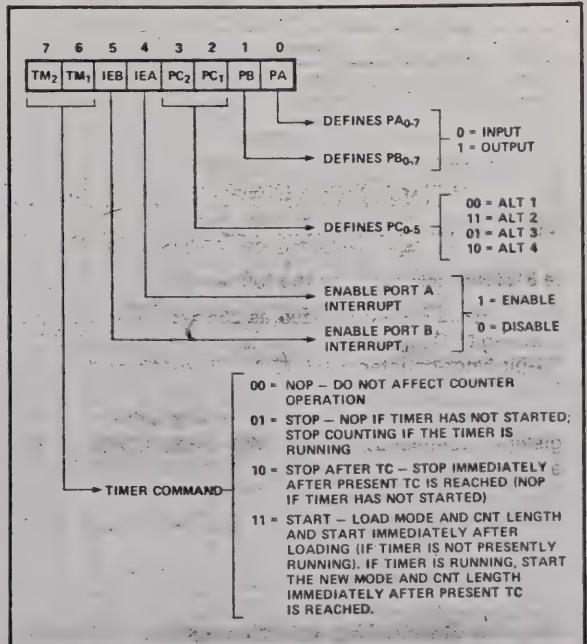


Figure 5. Command Register Bit Assignment



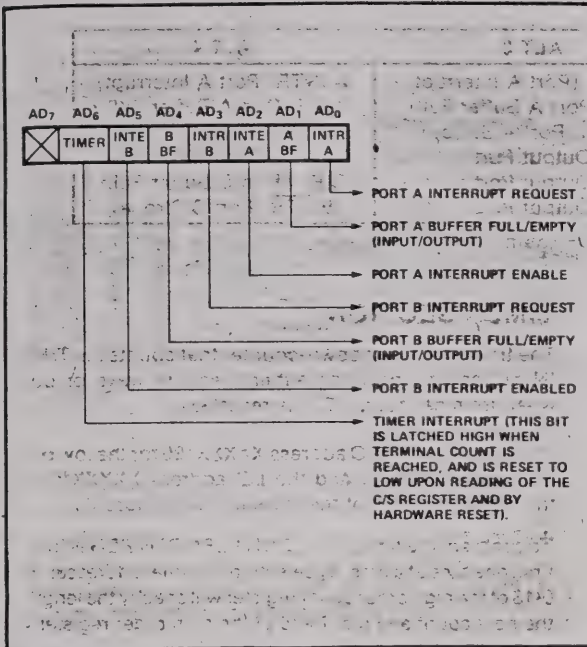


Table 2. Port Control Assignment

Pin	ALT 1	ALT 2	ALT 3	ALT 4
PC0	Input Port	Output Port	A INTR (Port A Interrupt)	A INTR (Port A Interrupt)
PC1	Input Port	Output Port	A BF (Port A Buffer Full)	A BF (Port A Buffer Full)
PC2	Input Port	Output Port	A STB (Port A Strobe)	A STB (Port A Strobe)
PC3	Input Port	Output Port	Output Port	B INTR (Port B Interrupt)
PC4	Input Port	Output Port	Output Port	B BF (Port B Buffer Full)
PC5	Input Port	Output Port	Output Port	B STB (Port B Strobe)

Note in the diagram that when the I/O ports are programmed to be output ports, the contents of the output ports can still be read by a READ operation when appropriately addressed.

The outputs of the 8155H/8156H are "glitch-free" meaning that you can write a "1" to a bit position that was previously "1" and the level at the output pin will not change.

Note also that the output latch is cleared when the port enters the input mode. The output latch cannot be loaded by writing to the port if the port is in the input mode. The result is that each time a port mode is changed from input to output, the output pins will go low. When the 8155H/56H is RESET, the output latches are all cleared and all 3 ports enter the input mode.

When in the ALT 1 or ALT 2 modes, the bits of PORT C are structured like the diagram above in the simple input or output mode, respectively.

Reading from an input port with nothing connected to the pins will provide unpredictable results.

Figure 9 shows how the 8155H/8156H I/O ports might be configured in a typical MCS-85 system.

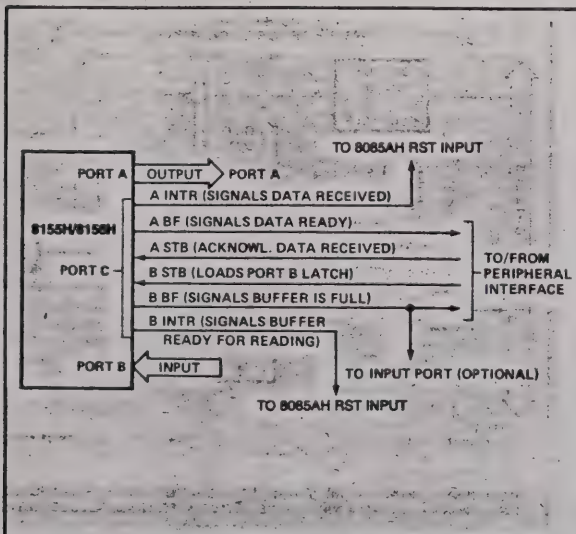


Figure 9. Example: Command Register = 00111001

TIMER SECTION

The timer is a 14-bit down-counter that counts the TIMER IN pulses and provides either a square wave or pulse when terminal count (TC) is reached.

The timer has the I/O address XXXXX100 for the low order byte of the register and the I/O address XXXXX101 for the high order byte of the register. (See Figure 7.)

To program the timer, the COUNT LENGTH REG is loaded first, one byte at a time, by selecting the timer addresses. Bits 0-13 of the high order count register will specify the length of the next count and bits 14-15 of the high order register will specify the timer output mode (see Figure 10). The value loaded into the count length register can have any value from 2H through 3FFFH in Bits 0-13.

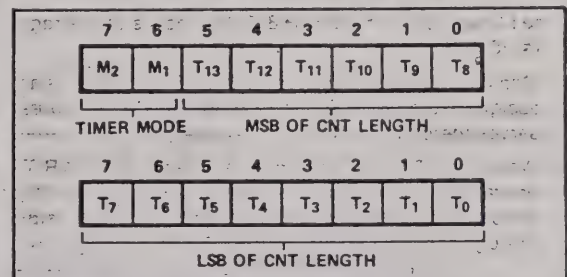


Figure 10. Timer Format

There are four modes to choose from: M2 and M1 define the timer mode, as shown in Figure 11:

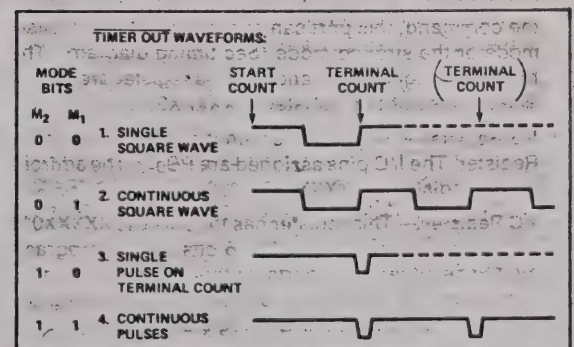


Figure 11. Timer Modes

Bits 6-7 (TM₂ and TM₁) of command register contents are used to start and stop the counter. There are four commands to choose from:

TM ₂	TM ₁	
0	0	NOP — Do not affect counter operation.
0	1	STOP — NOP if timer has not started; stop counting if the timer is running.
1	0	STOP AFTER TC — Stop immediately after present TC is reached (NOP if timer has not started)
1	1	START — Load mode and CNT length and start immediately after loading (if timer is not presently running). If timer is running, start the new mode and CNT length immediately after present TC is reached.

Note that while the counter is counting, you may load a new count and mode into the count length registers. Before the new count and mode will be used by the counter, you must issue a START command to the counter. This applies even though you may only want to change the count and use the previous mode.

In case of an odd-numbered count, the first half-cycle of the squarewave output, which is high, is one count longer than the second (low) half-cycle, as shown in Figure 12.

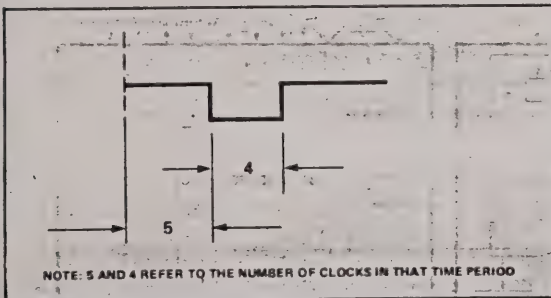


Figure 12. Asymmetrical Square-Wave Output Resulting from Count of 9

The counter in the 8155H is not initialized to any particular mode or count when hardware RESET occurs, but RESET does *stop* the counting. Therefore, counting cannot begin following RESET until a START command is issued via the C/S register.

Please note that the timer circuit on the 8155H/8156H chip is designed to be a square-wave timer, not an event counter. To achieve this, it counts down by two's twice in completing one cycle. Thus, its registers do not contain values directly representing the number of TIMER IN pulses received. You cannot load an initial value of 1 into the count register and cause the timer to operate, as its terminal count value is 10 (binary) or 2 (decimal). (For the detection of single pulses, it is suggested that one of the hardware interrupt pins on the 8085AH be used.) After the timer has started counting down, the values residing in the count registers can be used to calculate the actual number of TIMER IN pulses required to complete the timer cycle if desired. To obtain the remaining count, perform the following operations in order:

1. Stop the count
2. Read in the 16-bit value from the count length registers
3. Reset the upper two mode bits
4. Reset the carry and rotate right one position all 16 bits through carry
5. If carry is set, add 1/2 of the full original count (1/2 full count — 1 if full count is odd).

Note: If you started with an odd count and you read the count length register before the third count pulse occurs, you will not be able to discern whether one or two counts has occurred. Regardless of this, the 8155H/56H always counts out the right number of pulses in generating the TIMER OUT waveforms.

SOFTWARE REFERENCE MANUAL

HDOS SYSTEM

Chapter 4

HEATH ASSEMBLY LANGUAGE ASM

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WRITING ASSEMBLY LANGUAGE PROGRAMS

The Heath Assembly Language program (ASM) lets you use source (symbolic) programs using letters, numbers, and symbols that are meaningful as they are abbreviated in English statements. These source programs must be generated with the Heath Text Editor (EDIT). ASM assembles the source program into a listing and an object program in absolute binary format executable by your Computer.

This Manual assumes that you are already familiar with the writing of assembly language programs. Also, because of the many cross-references in this Section, we recommend that you read all of this Section to get a good “feel” for ASM.

ASM is designed to produce programs which run in an H8/H89 system; therefore, it assembles 8080 symbolic assembly code. When it is used with 16K of memory, ASM provides for approximately 350 user-defined symbols.

This Software reference Manual presumes that you have read the Operation Manual and are familiar with the 8080 instruction set, I/O formats, memory formats, and front panel configuration. A thorough knowledge of these facts is vital to efficient assembly language programming.

THE CHARACTER SET

The Heath Assembly Language source program is composed of symbols, numbers, expressions, symbolic instructions, argument separators, assembly directives, and line terminators, all using ASCII characters. Those characters that are acceptable to ASM are listed below.

1. The letters A through Z (lower case letters are acceptable for quoted strings and comments).
2. The numerals 0 through 9.
3. The characters period (.) and dollar sign (\$), which are considered alphabetic.
4. The symbols:

: = % # () , ; " ' + - _ ! ?
5. BLANKS and TABS.

STATEMENTS

A source program is composed of a sequence of statements, designed to solve a problem. Each statement must be on a single line.

A statement is composed of up to four fields, identified by the order of appearance and separated by BLANKS and TABS. The four fields are:

LABEL	OPCODE	OPERAND	COMMENT
-------	--------	---------	---------

The label on comment fields are optional. The opcode and operand fields are interdependent; either may be omitted, depending upon the contents of the other.

The Label Field

The label field always starts in column one. A label is a user-defined symbol assigned the current value of the memory location counter. It is a symbolic means of referring to a specific memory location within a program. Most statements do not require a label. If you do not want a label, column one must be left blank or contain a TAB. Although the label is usually used to allow symbolic reference to the address of the labeled instruction, the SET and EQU pseudos make special use of the label field.

A label must start with an alphabetic character, and it consists entirely of alphabetic or numeric characters. The maximum length of a label is 7 characters. Note that the characters "\$" and "." are considered alphabetic. Therefore, the following are valid labels.

```
A A3 . C9D4 START .. $END END!PGM
```

For example, if the current location counter is set to 042 200 and the statement

```
START    MOV A,B
```

is the next statement, the assembler assigns the value 042 200 to the label START. Subsequent references to START refer to location 042 200.

The Opcode Field

All statements (except the comment statements) must have an opcode field. The opcode field need not be located in any particular column. However, it must be separated from the label field by at least one blank or TAB. If no label is specified, the opcode field may start in or after column 2.

The opcode is either an instruction mnemonic or an assembler directive. When the entry in the opcode field is an instruction mnemonic, it specifies a machine operation to be performed on any following operands. When it is an assembler directive, it specifies certain functions or actions to be performed by the assembler during program assembly.

The opcode field is terminated by a blank, a TAB, or the end of a line.

The Operand Field

The operand field follows the opcode field and must be separated from it by at least one blank or TAB. Not all opcodes require operands. The operand contains information used by a machine instruction or, in the case of assembler directives (pseudo opcodes or pseudo ops), it contains information to be used by the pseudo op.

Operands may be symbols, expressions, or numbers. When multiple operands appear with a statement, each is separated from the next by a comma. An operand may be followed by a comment.

The operand field is terminated by a blank or TAB when followed by a comment, or by the end of a line when the operand ends the assembly statement. For example,

```
START    MOV A,B    THIS IS A COMMENT
```

The TAB between START and MOV terminates the label field; the blank between MOV and A,B terminates the opcode field and begins the operand field. The comma separates the operands A and B and the TAB terminates the operand field and begins the comment field.

The Comment Field

The comment field follows the operand field, or the opcode field if no operand field is present. It must be separated from its preceding field by at least one blank or TAB. The comment field is not processed by the assembler and it is designed to contain documentary information. The comment field is optional and may contain any printing ASCII character. All other characters, even those with special significance to the assembler, are ignored by the assembler when used in the comment field.

A statement with an asterisk (*) in column one is taken as a comment statement and is not otherwise processed by the assembler. A totally blank line is also taken as a comment.

Format Control

The format of an assembly language program is controlled by the blank and TAB characters. Format control is primarily used to produce a program which is easily read. Format control has no effect on the assembly process of the source program. The following two statements are interpreted identically. The first one uses blanks and the second uses TABS.

```
START MOV A,B  THIS IS A COMMENT
START  MOV A,B   THIS IS A COMMENT
```

OPERAND EXPRESSIONS

Except when the opcode is a machine instruction requiring that an 8080 register be specified as the operand, all operand fields may be coded as operand expressions. Such operand expressions are made up of integers, symbols, a special origin symbol, and character strings which may be combined, using certain operators. The operand may also be the origin symbol. The expressions are said to be made up of operators and tokens. No parentheses are allowed nor is any operator precedence recognized. Therefore, evaluation is strictly left to right. The result of any expression must fall between $-32,767$ and $65,534$.

Operators

ASM recognizes 5 operators. They are:

- +
 - −
 - *
 - /
 - −
- Addition of an integer arithmetic expression.
Subtraction of an integer arithmetic expression.
Multiplication of an integer arithmetic expression.
Division of an integer arithmetic expression.
(unary) negation of a standard integer arithmetic expression.

Note, the unary minus is valid only as the first character in an expression. The following are examples of legitimate assembler operand expressions.

```
3+5
−2    (unary)
1+2*3
```

Note that the last example evaluates to 9 rather than 7, as the **assembler does not recognize any operator precedence**. Therefore, it evaluates the expression from left to right.

Tokens

Heath Assembly Language recognizes four different tokens: integers, symbols, character strings, and the origin symbol. Each of these tokens has the limitations described in the following sections.

INTEGERS

Decimal integers ranging from 0 to 65,535 are allowed, but no decimal place may be specified. The radix of an integer expressions is assumed to be decimal. However, you may specify binary, octal, offset octal, decimal, or hexadecimal. Specify them by using a post-radix symbol following the integer expression.

B	Binary
O or Q	Octal
D	Decimal
H	Hexadecimal
A	Offset Octal

For example:

<u>EXPRESSION</u>	<u>RADIX</u>	<u>DECIMAL VALUE</u>
000 00011B	Binary	3
160Q	Octal (also 160O)	112
3200	Decimal (also 3200D)	3200
77000A	Offset octal	16128
021AH	Hexadecimal	282

<u>LEGAL INTEGER EXPRESSIONS</u>	<u>ILLEGAL INTEGER EXPRESSIONS</u>	<u>COMMENTS</u>
232	232.1	Decimals may not be specified
10111B	226B	Not a binary number
177Q	888	Not an octal number
A1FH	21C	No hex radix specified

If an integer expression evaluates to less than -32,767, or greater than 65,534, an error code is flagged.

SYMBOLS

An expression may contain any user defined symbol. Although most symbols do not need to be defined sequentially before the referencing statement, some pseudo operators require all their operand symbols to be defined in earlier statements in the program. Such operators are said to require "pass one evaluation" and are documented in "The 8080 Opcodes" (Page 4-10). All symbols must consist of legal ASM characters.

The # Symbol

If the pound sign (#) is the first character in an expression, the expression is evaluated as a 16-bit expression. After the expression is evaluated, the resultant value is masked to an 8-bit equivalent. Once this is done, a 16-bit operand may be referenced in an instruction requiring 8 bits without causing an overflow (V) error. For example:

```
MVI    H, ADDR/256
MVI    L, #ADDR      (HL) = 16 bit address
```

In this example, the first line of code loads the H and L register pair (16-bit register) with the binary value associated with the label "ADDR" divided by 256. The second line of code immediately loads the L register (an 8-bit register) with the lower 8-bits of the binary value equated to the symbol ADDR in the symbol table. This process does not cause an overflow error, as the 16-bit binary equivalent of ADDR is masked to the least significant 8-bits before it is moved into the 8-bit L register.

CHARACTER STRING

A character string consisting of one or two legal characters may be used as a token in an ASM expression. Such a character string is enclosed in a single quote (apostrophe). For example:

```
'A'      The character A (Value 101Q)
'GL'     The character string GL (Value 107 114A)
' " '    The character quotation mark (Value 042Q)
```


THE ORIGIN SYMBOL (*)

The current value of the origin counter may be referenced with the special symbol asterisk (*). NOTE: The assembler decides from the expression context whether the asterisk (*) represents the origin counter or is the multiplication operator. For example, the program

```
      ORG      10
A      EQU      ***
```

defines the symbol A to have the value 100. The first statement, “ORG 10,” sets the origin counter to the value 10. In the second statement, the label A is equated with the first asterisk, which the assembler presumes to be the symbol for the origin counter. This is multiplied by the third symbol, which the assembler also presumes to be the origin symbol. However, the middle asterisk is taken as the multiplication operator.

THE 8080 OPCODES†

Heath Assembly Language supports the standard 8080 machine opcodes. A review of the 8080 instruction set is presented on the following pages. Included in this review is a discussion of instruction and data formats, addressing modes, conditions flags, the symbols or abbreviations used in describing the 8080 instruction set, and the discussion of the format used to describe each instruction.

The 8080 instruction set includes five different types of instructions:

- **Data Transfer Group** — move data between registers or between memory and registers.
- **Arithmetic Group** — add, subtract, increment, or decrement data in registers or in memory.
- **Logical Group** — AND, OR, EXCLUSIVE-OR, compare, rotate, or complement data in registers or in memory.
- **Branch Group** — conditional and unconditional jump instructions, subroutine call instructions, and return instructions.
- **Stack, I/O and Machine Control Group** — includes I/O instructions, as well as instructions for maintaining the stack and internal control flags.

†Portions of this section are reprinted with the permission of Intel Corporation (Copyright, 1976).

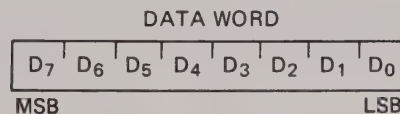
Terms, Symbols, & Nomenclature

INSTRUCTION AND DATA FORMATS

Memory for the 8080 is organized into 8-bit quantities called bytes. Each byte has a unique 16-bit binary address corresponding to its sequential position in memory.

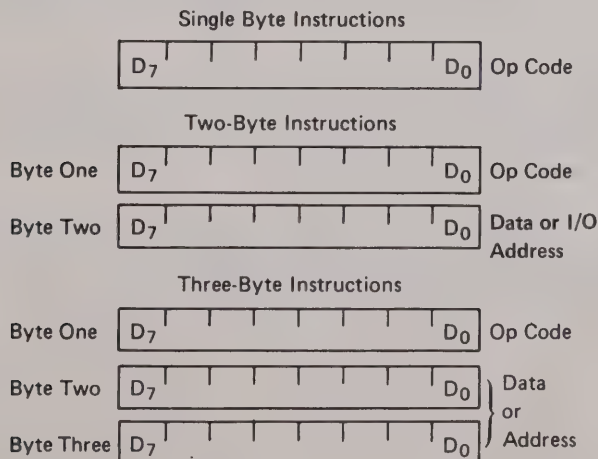
The 8080 can directly address up to 65,535 bytes of memory, which may consist of both read-only memory (ROM) elements and random-access memory (RAM) elements (read/write memory).

Data in the 8080 is stored in the form of 8-bit binary integers:



When a register or data word contains a binary number, it is necessary to establish the order in which the bits of the number are written. In the Intel 8080, BIT 0 is referred to as the **Least Significant Bit (LSB)**, and BIT 7 (of an 8-bit number) is referred to as the **Most Significant Bit (MSB)**.

The 8080 program instructions may be one, two, or three bytes in length. Multiple byte instructions must be stored in successive memory locations; the address of the first byte is always used as the address of the instructions. The exact instruction format will depend on the particular operation to be executed.



ADDRESSING MODES

Often, the data that is to be operated on is stored in memory. When multi-byte numeric data is used, the data, like instructions, is stored in successive memory locations with the least significant byte first, followed by increasingly significant bytes. The 8080 has four different modes for addressing data stored in memory or in registers:

- **Direct** — Bytes 2 and 3 of the instruction contain the exact memory address of the data item (the low-order bits of the address are in byte 2, the high-order bits in byte 3).
- **Register** — Specifies the register or register pair in which the data is located.
- **Register Indirect** — Specifies a register pair which contains the memory address where the data is located (the high-order bits of the address are in the first register of the pair, the low-order bits in the second).
- **Immediate** — Contains the data itself. This is either an 8-bit quantity or a 16-bit quantity (least significant byte first, most significant byte second).

Unless directed by an interrupt or branch instruction, the execution of instructions proceeds through consecutively increasing memory locations. A branch instruction can specify the address of the next instruction to be executed in one of two ways:

- **Direct** — The branch instruction contains the address of the next instruction to be executed. (Except for the “RST” instruction, byte 2 contains the low-order address and byte 3 the high-order address.)
- **Register Indirect** — The branch instruction indicates a register pair which contains the address of the next instruction to be executed. (The high-order bits of the address are in the first register of the pair, the low-order bits in the second.)

The RST instruction is a special 1-byte call instruction (usually used during interrupt sequences). RST includes a 3-bit field; program control is transferred to the instruction whose address is eight times the contents of this 3-bit field.

CONDITION FLAGS

There are five condition flags associated with the execution of instructions on the 8080. They are Zero, Sign, Parity, Carry, and Auxiliary Carry, and are each represented by a 1-bit register in the CPU. A flag is "set" by forcing the bit to 1; and "reset" by forcing the bit to 0.

Unless indicated otherwise, when an instruction affects a flag, it affects it in the following manner.

Zero: If the result of an instruction has the value 0, this flag is set. Otherwise it is reset.

Sign: If the most significant bit of the result of the operation has the value 1, this flag is set. Otherwise it is reset.

Parity If the modulo 2 sum of the bits of the result of the operation is 0 (i. e., if the result has even parity), this flag is set. Otherwise it is reset (i. e., if the result has odd parity).

Carry: If the instruction resulted in a carry (from addition), or a borrow (from subtraction or a comparison) out of the high-order bit, this flag is set. Otherwise it is reset.

Auxiliary Carry: If the instruction caused a carry out of bit 3 and into bit 4 of the resulting value, the auxiliary carry is set. Otherwise it is reset. This flag is affected by single precision additions, subtractions, increments, decrements, comparisons, and logical operations, but is principally used with additions and increments preceding a DAA (Decimal Adjust Accumulator) instruction.

Symbols and Abbreviations

The following symbols and abbreviations are used in the subsequent description of the 8080 instructions:

SYMBOLS	MEANING
accumulator	Register A
addr	16-bit address quantity
data	8-bit data quantity
data 16	16-bit data quantity
byte 2	The second byte of the instruction
byte 3	The third byte of the instruction
port	8-bit address of an I/O device
r, r1, r2	One of the registers A,B,C,D,E,H,L
DDD, SSS	The bit pattern designating one of the registers A, B, C, D, E, H, L (DDD = destination, SSS = source):

DDD or SSS	REGISTER NAME
111	A
000	B
001	C
010	D
011	E
100	H
101	L

rp One of the register pairs:

B represents the B, C pair with B as the high-order register and C as the low-order register;

D represents the D, E pair with D as the high-order register and E as the low-order register;

H represents the H, L pair with H as the high-order register and L as the low-order register;

SP represents the 16-bit stack pointer register.

RP The bit pattern designating one of the register pairs B, D, H, SP:

RP	REGISTER PAIR
00	B-C
01	D-E
10	H-L
11	SP

rh The first (high-order) register of a designated register pair.

rl The second (low-order) register of a designated register pair.

PC 16-bit program counter register (PCH and PCL are used to refer to the high-order and low-order 8-bits respectively).

SP 16-bit stack pointer register (SPH and SPL are used to refer to the high-order and low-order 8-bits respectively).

rm Bit m of the register r (bits are numbered 7 through 0 from left to right).

Z, S, P, The condition flags:
Cy, AC

Zero,
Sign,
Parity,
Carry,
and Auxiliary Carry,
respectively.

NOTE, ASM recognizes the E as well as the Z defining the zero bit. Therefore, JZ (jump zero) or JE (jump equal) are both valid op-codes.

() The contents of the memory location or registers enclosed in the parentheses.

← “Is transferred to”

∧ Logical AND

⊕ Exclusive OR

∨ Inclusive OR

⊕ Addition

− Two’s complement subtraction

* Multiplication

↔ “Is exchanged with”

— The one’s complement (e. g., \bar{A})

n The restart number 0 through 7

NNN The binary representation 000 through 111
for restart number 0 through 7, respectively.

Description Format

The following pages provide a detailed description of the instruction set of the 8080. Each instruction is described in the following manner:

1. The ASM format, consisting of the opcode and operand fields, is printed in **BOLDFACE** on the left side of the first line.
2. The name of the instruction is enclosed in parentheses at the center of the first line.
3. The next line(s) contain a symbolic description of the operation of the instruction.

4. This is followed by a narrative description of the operation of the instruction.
5. The following line(s) contain the binary fields and patterns that comprise the machine instruction.
6. The last two lines contain incidental information about the execution of the instruction. The number of machine cycles and states required to execute the instruction are listed first. If the instruction has two possible execution times, as in a conditional jump, both times will be listed, separated by a slash. Next, any significant data addressing modes (see "Addressing Modes," Page 4-12) are listed. The last line lists any of the five Flags that are affected by the execution of the instruction.

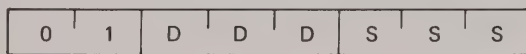
Data Transfer Group

This group of instructions transfers data to and from registers and memory. **Condition flags are not affected** by any instruction in this group.

MOV r1, r2 (Move Register)

$(r1) \leftarrow (r2)$

The content of register r2 is moved to register r1.



Cycles: 1

Addressing: register

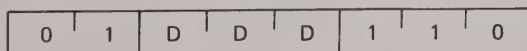
States: 5

Flags: none

MOV r, M (Move from memory)

$(r) \leftarrow ((H) (L))$

The content of the memory location whose address is in registers H and L is moved to register r.



Cycles: 2

Addressing: reg. indirect

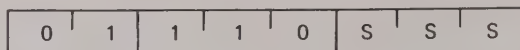
States: 7

Flags: none

MOV M, r (Move to memory)

$((H) (L)) \leftarrow (r)$

The content of register r is moved to the memory location whose address is in registers H and L.



Cycles: 2

States: 7

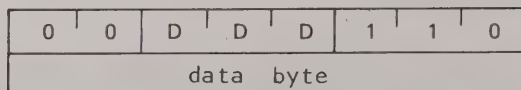
Addressing: reg. indirect

Flags: none

MVI r, data (Move to register immediate)

$(r) \leftarrow (\text{byte } 2)$

The content of byte 2 of the instruction is moved to register r.



Cycles: 2

States: 7

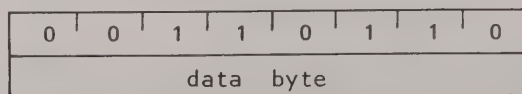
Addressing: immediate

Flags: none

MVI M, data (Move to memory immediate)

$((H) (L)) \leftarrow (\text{byte } 2)$

The content of byte 2 of the instruction is moved to the memory location whose address is in registers H and L.



Cycles: 3

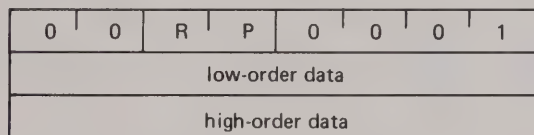
States: 10

Addressing: immed./reg.
indirect

Flags: none

LXI rp, data 16 (Load register pair immediate) $(rh) \leftarrow (\text{byte } 3),$ $(rl) \leftarrow (\text{byte } 2)$

Byte 3 of the instruction is moved into the high-order register (rh) of the register pair rp. Byte 2 of the instruction is moved into the low-order register (rl) of the register pair rp.



Cycles: 3

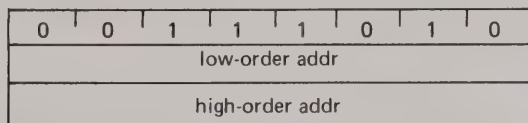
Addressing: immediate

States: 10

Flags: none

LDA addr (Load Accumulator direct) $(A) \leftarrow ((\text{byte } 3) (\text{byte } 2))$

The content of the memory location, whose address is specified in byte 2 and byte 3 of the instruction, is moved to register A.



Cycles: 4

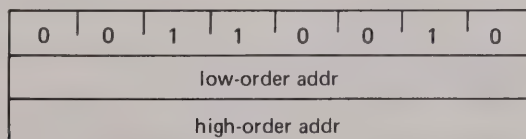
Addressing: direct

States: 13

Flags: none

STA addr (Store accumulator direct) $((\text{byte } 3) (\text{byte } 2)) \leftarrow (A)$

The content of the accumulator is moved to the memory location whose address is specified in byte 2 and byte 3 of the instruction.



Cycles: 4

Addressing: direct

States: 13

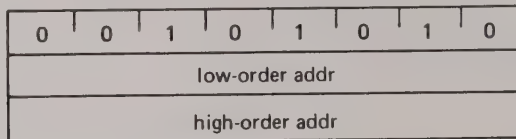
Flags: none

LHLD addr (Load H and L direct)

$(L) \leftarrow ((\text{byte } 3) (\text{byte } 2))$

$(H) \leftarrow ((\text{byte } 3) (\text{byte } 2) + 1)$

The content of the memory location whose address is specified in byte 2 and byte 3 of the instruction is moved to register L. The content of the memory location at the succeeding address is moved to register H.



Cycles: 5
States: 16

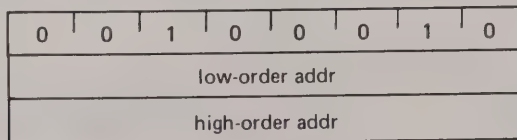
Addressing: direct
Flags: none

SHLD addr (Store H and L direct)

$((\text{byte } 3) (\text{byte } 2)) \leftarrow (L)$

$((\text{byte } 3) (\text{byte } 2) + 1) \leftarrow (H)$

The content of register L is moved to the memory location whose address is specified in byte 2 and byte 3. The content of register H is moved to the succeeding memory location.



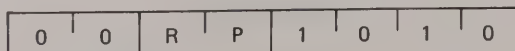
Cycles: 5
States: 16

Addressing: direct
Flags: none

LDAX rp (Load accumulator indirect)

$(A) \leftarrow ((rp))$

The content of the memory location whose address is in the register pair rp is moved to register A. NOTE: Only register pairs $rp = B$ (registers B and C) or $rp = D$ (registers D and E) may be specified.

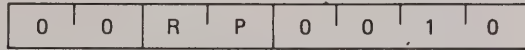


Cycles: 2
States: 7

Addressing: reg. indirect
Flags: none

STAX rp (Store accumulator indirect)
$$((rp)) \leftarrow (A)$$

The content of register A is moved to the memory location whose address is in the register pair rp. NOTE: Only register pairs rp = B (registers B and C) or rp = D (registers D and E) may be specified.



Cycles: 2

Addressing: reg. indirect

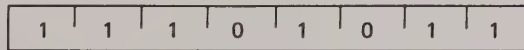
States: 7

Flags: none

XCHG (Exchange H and L with D and E)
$$(H) \longleftrightarrow (D)$$

$$(L) \longleftrightarrow (E)$$

The contents of registers H and L are exchanged with the contents of registers D and E.



Cycles: 1

Addressing: register

States: 4

Flags: none

Arithmetic Group

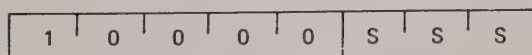
This group of instructions performs arithmetic operations on data in registers and memory.

Unless indicated otherwise, all instructions in this group affect the Zero, Sign, Parity, Carry, and Auxiliary Carry flags according to the standard rules.

All subtraction operations are performed via two's complement arithmetic and set the carry flag to one to indicate a borrow and clear it to indicate no borrow.

ADD r (Add Register)
$$(A) \leftarrow (A) + (r)$$

The content of register r is added to the content of the accumulator. The result is placed in the accumulator.



Cycles: 1

Addressing: register

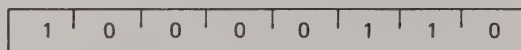
States: 4

Flags: Z,S,P,CY,AC

ADD M (Add memory)

$$(A) \leftarrow (A) + ((H) (L))$$

The content of the memory location whose address is contained in the H and L registers is added to the content of the accumulator. The result is placed in the accumulator.



Cycles: 2

States: 7

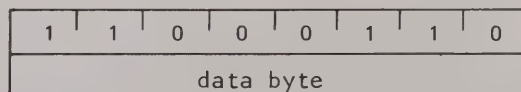
Addressing: reg. indirect

Flags: Z,S,P,CY,AC

ADI DATA (add immediate)

$$(A) \leftarrow (A) + (\text{byte 2})$$

The content of the second byte of the instruction is added to the content of the accumulator. The result is placed in the accumulator.



Cycles: 2

States: 7

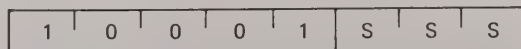
Addressing: immediate

Flags: Z,S,P,CY,AC

ADC r (Add Register with carry)

$$(A) \leftarrow (A) + (r) + (CY)$$

The content of register r and the content of the carry bit are added to the content of the accumulator. The result is placed in the accumulator.



Cycles: 1

States: 4

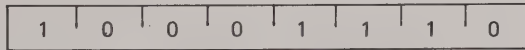
Addressing: register

Flags: Z,S,P,CY,AC

ADC M (Add memory with carry)

$$(A) \leftarrow (A) + ((H) (L)) + (CY)$$

The content of the memory location whose address is contained in the H and L registers and the content of the CY flag are added to the accumulator. The result is placed in the accumulator.



Cycles: 2

Addressing: reg. indirect

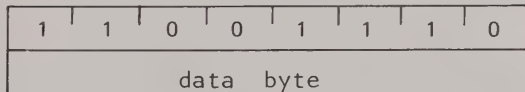
States: 7

Flags: Z,S,P,CY,AC

ACI data (Add immediate with carry)

$$(A) \leftarrow (A) + (\text{byte 2}) + (CY)$$

The content of the second byte of the instruction and the content of the CY flag are added to the contents of the accumulator. The result is placed in the accumulator.



Cycles: 2

Addressing: immediate

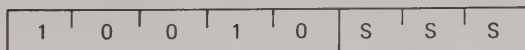
States: 7

Flags: Z,S,P,CY,AC

SUB r (Subtract Register)

$$(A) \leftarrow (A) - (r)$$

The content of register r is subtracted from the content of the accumulator. The result is placed in the accumulator.



Cycles: 1

Addressing: register

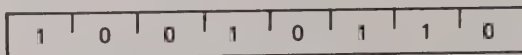
States: 4

Flags: Z,S,P,CY,AC

SUB M (Subtract memory)

$$(A) \leftarrow (A) - ((H) (L))$$

The content of the memory location whose address is contained in the H and L registers is subtracted from the content of the accumulator. The result is placed in the accumulator.



Cycles: 2

States: 7

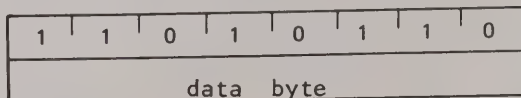
Addressing: reg. indirect

Flags: Z,S,P,CY,AC

SUI DATA (Subtract immediate)

$$(A) \leftarrow (A) - (\text{byte } 2)$$

The content of the second byte of the instruction is subtracted from the content of the accumulator. The result is placed in the accumulator.



Cycles: 2

States: 7

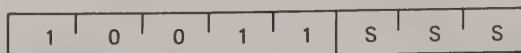
Addressing: immediate

Flags: Z,S,P,CY,AC

SBB r (Subtract Register with borrow)

$$(A) \leftarrow (A) - (r) - (CY)$$

The content of register r and the content of the CY flag are both subtracted from the accumulator. The result is placed in the accumulator.



Cycles: 1

States: 4

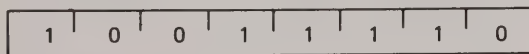
Addressing: register

Flags: Z,S,P,CY,AC

SBB M (Subtract memory with borrow)

$$(A) \leftarrow (A) - ((H) (L)) - (CY)$$

The content of the memory location whose address is contained in the H and I registers and the content of the CY flag are both subtracted from the accumulator. The result is placed in the accumulator.



Cycles: 2

Addressing: reg. indirect

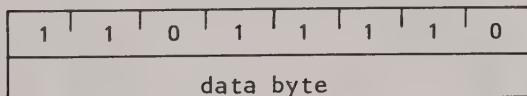
States: 7

Flags: Z,S,P,CY,AC

SBI data (Subtract immediate with borrow)

$$(A) \leftarrow (A) - (\text{byte 2}) - (CY)$$

The contents of the second byte of the instruction and the contents of the CY flag are both subtracted from the accumulator. The result is placed in the accumulator.



Cycles: 2

Addressing: immediate

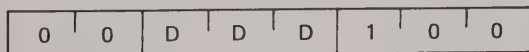
States: 7

Flags: Z,S,P,CY,AC

INR r (Increment Register)

$$(r) \leftarrow (r) + 1$$

The content of register r is incremented by one. NOTE: All condition flags **except** CY are affected.



Cycles: 1

Addressing: register

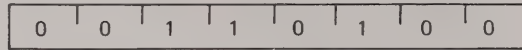
States: 5

Flags: Z,S,P,AC

INR M (Increment memory)

$$((H) (L)) \leftarrow ((H) (L)) + 1$$

The content of the memory location whose address is contained in the H and L registers is incremented by one. NOTE: All condition flags **except CY** are affected.



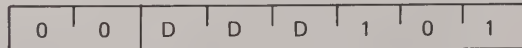
Cycles: 3
States: 10

Addressing: reg. indirect
Flags: Z,S,P,AC

DCR r (Decrement Register)

$$(r) \leftarrow (r) - 1$$

The content of register r is decremented by one. NOTE: All condition flags **except CY** are affected.



Cycles: 1
States: 5

Addressing: register
Flags: Z,S,P,AC

DCR M (Decrement memory)

$$((H) (L)) \leftarrow ((H) (L)) - 1$$

The content of the memory location whose address is contained in the H and L registers is decremented by one. NOTE: All condition flags **except CY** are affected.



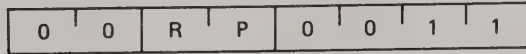
Cycles: 3
States: 10

Addressing: reg. indirect
Flags: Z, S, P, AC

INX rp (Increment register pair)

$$(rh) (rl) \leftarrow (rh) (rl) + 1$$

The content of the register pair rp is incremented by one. NOTE: **No condition flags are affected.**



Cycles: 1

Addressing: register

States: 5

Flags: none

DCX rp (Decrement register pair)

$$(rh) (rl) \leftarrow (rh) (rl) - 1$$

The content of register pair rp is decremented by one. NOTE: **No condition flags are affected.**



Cycles: 1

Addressing: register

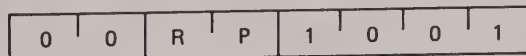
States: 5

Flags: none

DAD rp (Add register pair to H and L)

$$(H) (L) \leftarrow (H) (L) + (rh) (rl)$$

The content of register pair rp is added to the content of the register pair H and L. The result is placed in register pair H and L. NOTE: **Only the CY flag is affected.** It is set if there is a carry out of the double precision add; otherwise it is reset.



Cycles: 3

Addressing: register

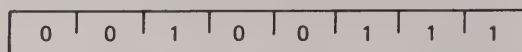
States: 10

Flags: CY

DAA (Decimal Adjust Accumulator)

The eight-bit number in the accumulator is adjusted to form two 4-bit Binary-Coded-Decimal digits by the following process:

1. If the value of the least significant 4 bits of the accumulator is greater than 9 **or** if the AC flag is set, 6 is added to the accumulator.
2. If the value of the most significant 4 bits of the accumulator is now greater than 9, **or** if the CY flag is set, 6 is added to the most significant 4 bits of the accumulator.



Cycles:	1
States:	4
Flags:	Z,S,P,CY,AC

Logical Group:

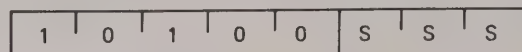
This group of instructions performs logical (Boolean) operations on data in registers and memory and on condition flags.

Unless indicated otherwise, all instructions in this group affect the Zero, Sign, Parity, Auxiliary Carry, and Carry flags according to the standard rules.

ANA r (AND Register)

$$(A) \leftarrow (A) \wedge (r)$$

The content of register r is logically anded with the content of the accumulator. The result is placed in the accumulator. **The CY flag is cleared.**

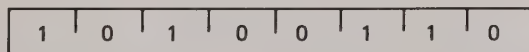


Cycles:	1	Addressing:	register
States:	4	Flags:	Z,S,P,CY,AC

ANA M (AND memory)

$$(A) \leftarrow (A) \wedge ((H) (L))$$

The contents of the memory location whose address is contained in the H and L registers is logically anded with the content of the accumulator. The result is placed in the accumulator. **The CY flag is cleared.**



Cycles: 2

Addressing: reg. indirect

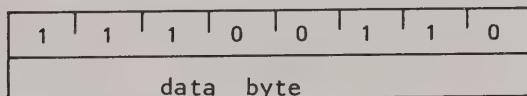
States: 7

Flags: Z,S,P,CY,AC

ANI data (AND immediate)

$$(A) \leftarrow (A) \wedge (\text{byte } 2)$$

The content of the second byte of the instruction is logically anded with the contents of the accumulator. The result is placed in the accumulator. **The CY and AC flags are cleared.**



Cycles: 2

Addressing: immediate

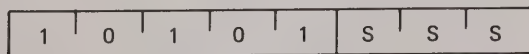
States: 7

Flags: Z,S,P,CY,AC

XRA r (Exclusive OR Register)

$$(A) \leftarrow (A) \nabla (r)$$

The content of register r is exclusive-OR'd with the content of the accumulator. The result is placed in the accumulator. **The CY and AC flags are cleared.**



Cycles: 1

Addressing: register

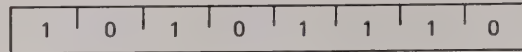
States: 4

Flags: Z,S,P,CY,AC

XRA M (Exclusive OR Memory)

$$(A) \leftarrow (A) \nabla ((H) (L))$$

The content of the memory location whose address is contained in the H and L registers is exclusive-OR'd with the content of the accumulator. The result is placed in the accumulator. **The CY and AC flags are cleared.**



Cycles: 2

States: 7

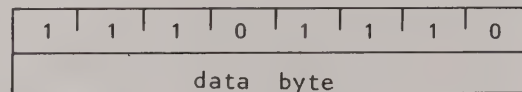
Addressing: reg. indirect

Flags: Z,S,P,CY,AC

XRI data (Exclusive OR immediate)

$$(A) \leftarrow (A) \nabla (\text{byte } 2)$$

The content of the second byte of the instruction is exclusive-OR'd with the content of the accumulator. The result is placed in the accumulator. **The CY and AC flags are cleared.**



Cycles: 2

States: 7

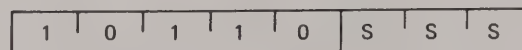
Addressing: immediate

Flags: Z,S,P,CY,AC

ORA r (OR Register)

$$(A) \leftarrow (A) \vee (r)$$

The content of register r is inclusive-OR'd with the content of the accumulator. The result is placed in the accumulator. **The CY and AC flags are cleared.**



Cycles: 1

States: 4

Addressing: register

Flags: Z,S,P,CY,AC

ORA M (OR memory)

$$(A) \leftarrow (A) \vee ((H) (L))$$

The content of the memory location whose address is contained in the H and L registers is inclusive-OR'd with the content of the accumulator. The result is placed in the accumulator. **The CY and AC flags are cleared.**



Cycles: 2

Addressing: reg. indirect

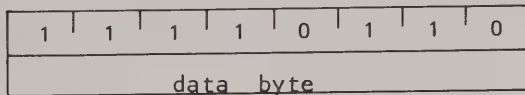
States: 7

Flags: Z,S,P,CY,AC

ORI data (OR Immediate)

$$(A) \leftarrow (A) \vee (\text{byte } 2)$$

The content of the second byte of the instruction is inclusive-OR'd with the content of the accumulator. The result is placed in the accumulator. **The CY and AC flags are cleared.**



Cycles: 2

Addressing: immediate

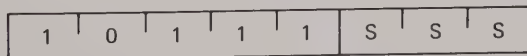
States: 7

Flags: Z,S,P,CY,AC

CMP r (Compare Register)

$$(A) - (r)$$

The content of register r is subtracted from the accumulator. The accumulator remains unchanged. The condition flags are set as a result of the subtraction. **The Z flag is set to 1 if (A) = (r). The CY flag is set to 1 if (A) < (r).**



Cycles: 1

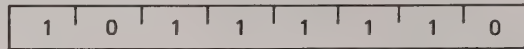
Addressing: register

States: 4

Flags: Z,S,P,CY,AC

CMP M (Compare memory) $(A) \leftarrow ((H) (L))$

The content of the memory location whose address is contained in the H and L registers is subtracted from the accumulator. The accumulator remains unchanged. The condition flags are set as a result of the subtraction. The Z flag is set to 1 if $(A) = ((H) (L))$. The CY flag is set to 1 if $(A) < ((H) (L))$.



Cycles: 2

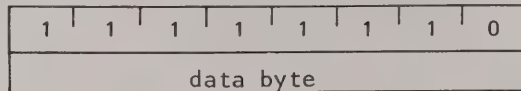
States: 7

Addressing: reg. indirect

Flags: Z,S,P,CY,AC

CPI data (Compare immediate) $(A) \leftarrow (\text{byte } 2)$

The content of the second byte of the instruction is subtracted from the accumulator. The condition flags are set by the result of the subtraction. The Z flag is set to 1 if $(A) = (\text{byte } 2)$. The CY flag is set to 1 if $(A) < (\text{byte } 2)$.



Cycles: 2

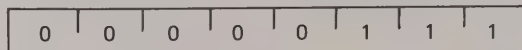
States: 7

Addressing: immediate

Flags: Z,S,P,CY,AC

RLC (Rotate left) $(A_{n+1}) \leftarrow (A_n); (A_0) \leftarrow (A_7)$ $(CY) \leftarrow (A_7)$

The content of the accumulator is rotated left one position. The low order bit and the CY flag are both set to the value shifted out of the high order bit position. **Only the CY flag is affected.**



Cycles: 1

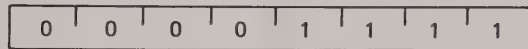
States: 4

Flags: CY

RRC (Rotate right)
$$(A_n) \leftarrow (A_{n-1}); (A_7) \leftarrow (A_0)$$

$$(CY) \leftarrow (A_0)$$

The content of the accumulator is rotated right one position. The high order bit and the CY flag are both set to the value shifted out of the low order bit position. **Only the CY flag is affected.**



Cycles: 1

States: 4

Flags: CY

RAL (Rotate left through carry)
$$(A_{n+1}) \leftarrow (A_n); (CY) \leftarrow (A_7)$$

$$(A_0) \leftarrow (CY)$$

The content of the accumulator is rotated left one position through the CY flag. The low order bit is set equal to the CY flag and the CY flag is set to the value shifted out of the high order bit. **Only the CY flag is affected.**



Cycles: 1

States: 4

Flags: CY

RAR (Rotate right through carry)
$$(A_n) \leftarrow (A_{n+1}); (CY) \leftarrow (A_0)$$

$$(A_7) \leftarrow (CY)$$

The content of the accumulator is rotated right one position through the CY flag. The high order bit is set to the CY flag and the CY flag is set to the value shifted out of the low order bit. **Only the CY flag is affected.**



Cycles: 1

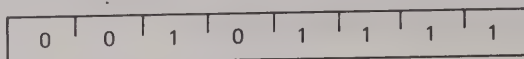
States: 4

Flags: CY

CMA (Complement accumulator)

$$(A) \leftarrow (A)$$

The contents of the accumulator are complemented (zero bits become 1, one bits become 0). **No flags are affected.**

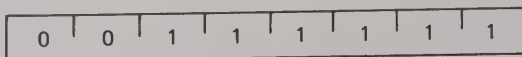


Cycles: 1
States: 4
Flags: none

CMC (Complement carry)

$$(CY) \leftarrow (\overline{CY})$$

The CY flag is complemented. **No other flags are affected.**

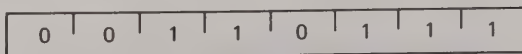


Cycles: 1
States: 4
Flags: CY

STC (Set carry)

$$(CY) \leftarrow 1$$

The CY flag is set to 1. **No other flags are affected.**



Cycles: 1
States: 4
Flags: CY

Branch Group

This group of instructions alter normal sequential program flow. **Condition flags are not affected** by any instruction in this group.

The two types of branch instructions are unconditional and conditional. Unconditional transfers simply perform the specified operation on register PC (the

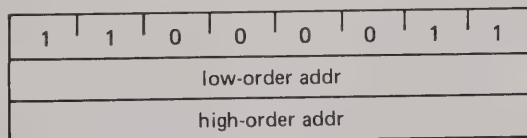
program counter). Conditional transfers examine the status of one of the four processor flags to determine if the specified branch is to be executed. The following conditions may be specified:

CONDITION	CCC	OCTAL
NE or NZ — not zero (Z=0)	000	0
E or Z — zero (Z=1)	001	1
NC — no carry (CY = 0)	010	2
C — carry (CY = 1)	011	3
PO — parity odd (P = 0)	100	4
PE — parity even (P = 1)	101	5
P — plus (S = 0)	110	6
M — minus (S = 1)	111	7

JMP addr (Jump)

(PC) ← (byte 3) (byte 2)

Control is transferred to the instruction whose address is specified in byte 3 and byte 2 of the current instruction.



Cycles: 3
States: 10

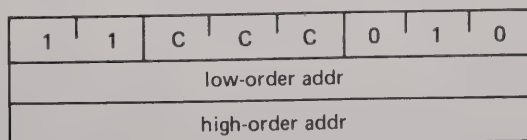
Addressing: immediate
Flags: none

JNE JNC JPO JP (Condition jump)
JE JC JPE JM

If (CCC),

(PC) ← (byte 3) (byte 2)

If the specified condition is true, control is transferred to the instruction whose address is specified in byte 3 and byte 2 of the current instruction. Otherwise, control continues sequentially.



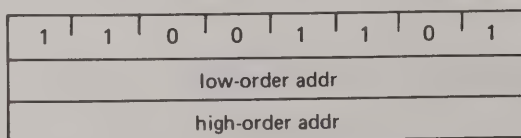
Cycles: 3
States: 10

Addressing: immediate
Flags: none

CALL addr (Call)

$((SP) - 1) \leftarrow (PCH)$
 $((SP) - 2) \leftarrow (PCL)$
 $(SP) \leftarrow (SP) - 2$
 $(PC) \leftarrow (\text{byte 3}) (\text{byte 2})$

The high-order eight bits of the next instruction address are moved to the memory location whose address is one less than the content of register SP. The low-order eight bits of the next instruction address are moved to the memory location whose address is two less than the content of register SP. The content of register SP is decremented by 2. Control is transferred to the instruction whose address is specified in byte 3 and byte 2 of the current instruction.



Cycles: 5

Addressing: immediate/reg.
indirect

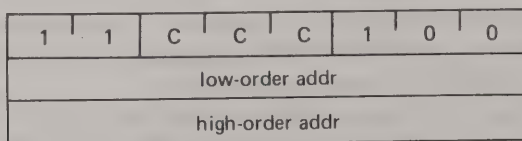
States: 17

Flags: none

CNE	CNC	CPO	CP	(Condition call)
CE	CC	CPE	CM	

If (CCC),
 $((SP) - 1) \leftarrow (PCH)$
 $((SP) - 2) \leftarrow (PCL)$
 $(SP) \leftarrow (SP) - 2$
 $(PC) \leftarrow (\text{byte 3}) (\text{byte 2})$

If the specified condition is true, the actions specified in the CALL instruction (see above) are performed; otherwise, control continues sequentially.



Cycles: 3/5

Addressing: immediate/reg.
indirect

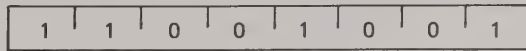
States: 11/17

Flags: none

RET (Return)

$(PCL) \leftarrow ((SP));$
 $(PCH) \leftarrow ((SP)) + 1;$
 $(SP) \leftarrow (SP) + 2;$

The content of the memory location whose address is specified in register SP is moved to the low-order eight bits of register PC. The content of the memory location whose address is one more than the content of register SP is moved to the high-order eight bits of register PC. The content of register SP is incremented by 2.



Cycles: 3

Addressing: reg. indirect

States: 10

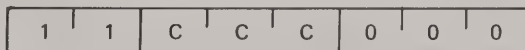
Flags: none

RNE RNC
RE RC (Conditional return)

If (CCC),

$(PCL) \leftarrow ((SP))$
 $(PCH) \leftarrow ((SP) + 1)$
 $(SP) \leftarrow (SP) + 2$

If the specified condition is true, the actions specified in the RET instruction (see above) are performed; otherwise, control continues sequentially.



Cycles: 1/3

Addressing: reg. indirect

States: 5/11

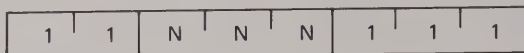
Flags: none

RST n (Restart)

$((SP) - 1) \leftarrow (PCH)$
 $((SP) - 2) \leftarrow (PCL)$
 $(SP) \leftarrow (SP) - 2$
 $(PC) \leftarrow 8 * (NNN)$

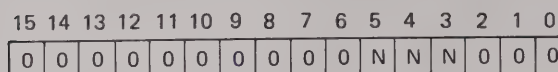
The high-order eight bits of the next instruction address are moved to the memory location whose address is one less than the content of register SP. The low-order eight bits of the next instruction address are moved to the memory location whose address is two less than the content of register SP.

The content of register SP is decremented by two. Control is transferred to the instruction whose address is eight times the content of NNN.



Cycles: 3
States: 11

Addressing: reg. indirect
Flags: none



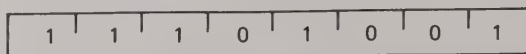
Program Counter After Restart

PCHL (Jump H and L indirect — move H and L to PC)

$(PCH) \leftarrow (H)$

$(PCL) \leftarrow (L)$

The content of register H is moved to the high-order eight bits of register PC. The content of register L is moved to the low-order eight bits of register PC.



Cycles: 1
States: 5

Addressing: register
Flags: none

Stack, I/O, and Machine Control Group

This group of instructions performs I/O, manipulates the Stack, and alters internal control flags. Unless otherwise specified, **condition flags are not affected by any instructions in this group.**

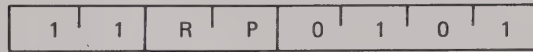
PUSH rp (Push)

$((SP) - 1) \leftarrow (rh)$

$((SP) - 2) \leftarrow (rl)$

$(SP) \leftarrow (SP) - 2$

The content of the high-order register of register pair (rp) is moved to the memory location whose address is one less than the content of register SP. The content of the low-order register of register pair (rp) is moved to the memory location whose address is two less than the content of register SP. The content of register SP is decremented by 2. **NOTE: Register pair (rp) = SP may not be specified.**



Cycles: 3

Addressing: reg. indirect

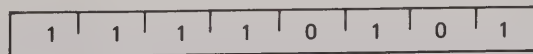
States: 11

Flags: none

PUSH PSW (Push processor status word)

$((SP) - 1) \leftarrow (A)$
 $((SP) - 2)_0 \leftarrow (CY), ((SP) - 2)_1 \leftarrow 1$
 $((SP) - 2)_2 \leftarrow (P), ((SP) - 2)_3 \leftarrow 0$
 $((SP) - 2)_4 \leftarrow (AC), ((SP) - 2)_5 \leftarrow 0$
 $((SP) - 2)_6 \leftarrow (Z), ((SP) - 2)_7 \leftarrow (S)$
 $(SP) \leftarrow (SP) - 2$

The content of register A is moved to the memory location whose address is one less than register SP. The contents of the condition flags are assembled into a processor status word and the word is moved to the memory location whose address is two less than the content of register SP. The content of register SP is decremented by two.



Cycles: 3

Addressing: reg. indirect

States: 11

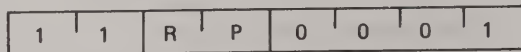
Flags: none

FLAG WORD

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
S	Z	0	AC	0	P	1	CY

POP rp (Pop)
$$\begin{aligned} (rl) &\leftarrow ((SP)) \\ (rh) &\leftarrow ((SP) + 1) \\ (SP) &\leftarrow (SP) + 2 \end{aligned}$$

The content of the memory location whose address is specified by the content of register SP is moved to the low-order register of register pair (rp). The content of the memory location whose address is one more than the content of register SP is moved to the high-order register of register pair (rp). The content of register SP is incremented by 2. **NOTE: Register pair (rp) = SP may not be specified.**

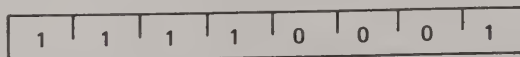


Cycles: 3
States: 10

Addressing: reg. indirect
Flags: none

POP PSW (Pop processor status word)
$$\begin{aligned} (CY) &\leftarrow ((SP))_0 \\ (P) &\leftarrow ((SP))_2 \\ (AC) &\leftarrow ((SP))_4 \\ (Z) &\leftarrow ((SP))_6 \\ (S) &\leftarrow ((SP))_7 \\ (A) &\leftarrow ((SP) + 1) \\ (SP) &\leftarrow (SP) + 2 \end{aligned}$$

The content of the memory location whose address is specified by the content of register SP is used to restore the condition flags. The content of the memory location whose address is one more than the content of register SP is moved to register A. The content of register SP is incremented by 2.

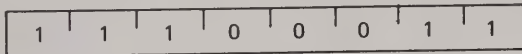


Cycles: 3
States: 10

Addressing: reg. indirect
Flags: Z,S,P,CY,AC

XTHL (Exchange stack top with H and L) $(L) \longleftrightarrow ((SP))$ $(H) \longleftrightarrow ((SP) + 1)$

The content of the L register is exchanged with the content of the memory location whose address is specified by the content of register SP. The content of the H register is exchanged with the content of the memory location whose address is one more than the content of register SP.



Cycles: 5

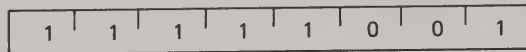
Addressing: reg. indirect

States: 18

Flags: none

SPHL (Move HL to SP) $(SP) \leftarrow (H) (L)$

The contents of registers H and L (16 bits) are moved to register SP.



Cycles: 1

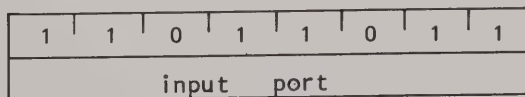
Addressing: register

States: 5

Flags: none

IN port (Input) $(A) \leftarrow (\text{data})$

The data placed on the eight bit bidirectional data bus by the specified port is moved to register A.



Cycles: 3

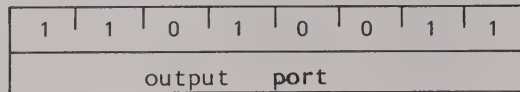
Addressing: direct

States: 10

Flags: none

OUT port (Output) $(\text{data}) \leftarrow (A)$

The content of register A is placed on the eight bit bidirectional data bus for transmission to the specified port.

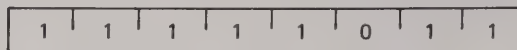


Cycles: 3
States: 10

Addressing: direct
Flags: none

EI (Enable interrupt)

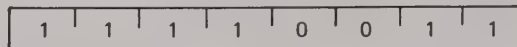
The interrupt system is enabled **following the execution of the next instruction.**



Cycles: 1
States: 4
Flags: none

DI (Disable interrupt)

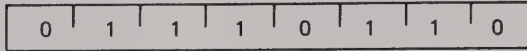
The interrupt system is disabled **immediately following the execution of the DI instruction.**



Cycles: 1
States: 4
Flags: none

HLT (Halt)

The processor is stopped. The registers and flags are unaffected.



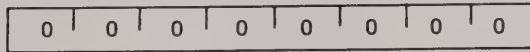
Cycles: 1

States: 7

Flags: none

NOP (No op)

No operation is performed. The registers and flags are unaffected.



Cycles: 1

States: 4

Flags: none

PSEUDO OPCODES/ASSEMBLER DIRECTIVES

The Heath Assembly Language supports several assembler directives or, as they are more commonly known, pseudo opcodes or simply pseudo ops. These opcodes are called “pseudo” because they are coded as machine operations. But as their alternate name (assembler directives) indicates, they represent commands to ASM and are not translated as instructions. Some pseudo ops affect the operation of the assembler. Others cause the assembler to generate constants into the generated object code.

Define Byte, DB

The DB pseudo defines byte contents. The DB pseudo is of the form:

```
Label DB iexp1, . . . . . ,iexpn
```

The integer expressions iexp1 through iexpn are expressions which evaluate to 8-bit values. For the DB pseudo, a long string can be substituted for an expression. The long string is a character string, delimited by single quotes ('), containing one or more characters. You can enclose a quote (') within a string by coding it as two single quotes. Each of the expressions is converted into an 8-bit binary number and stored in sequential memory locations. A few examples of the DB pseudo are:

CR	EQU	15Q
LF	EQU	12Q
	DB	1
	DB	2,3,4
	DB	1Q,CR,LF,'H8 BASIC',Q

In each case, the DB pseudo converts the expression into a single byte and stores it in the appropriate memory location. The DB pseudo recognized a character string as a series of expressions. Therefore, each character is converted into its ASCII binary equivalent and is stored in a sequential memory location.

Define Space, DS

The defined space pseudo (DS) reserves a block of memory during assembly.

The form of the DS pseudo is:

```
LABEL DS iexp COMMENT
```

This pseudo is used, for example, to set up a buffer area or to define any other storage area. The DS pseudo causes the assembler to reserve a number of bytes specified by the expression (iexp) in the operand. These bytes are not preset to any value. Therefore, you should not presume any special original contents. Programs using extensive buffer area should use the DS pseudo to declare this area. Using the DS pseudo significantly shortens the program load time. In the example

```
LINE DS 80 80 character input line buffer
```

an 80-character input buffer is reserved by a single statement.

Define Word, DW

The DW pseudo defines word constants. The form of the DW pseudo is:

```
LABEL DW iexpl, . . . . . , iexpn
```

The DW pseudo specifies one or more data words iexp through iexpn. Data words are **2-byte** values which are placed into memory space, low order byte first. NOTE: Strings greater than two characters long are not allowed when you are using the DW pseudo.

Conditional Assembly Pseudo Operators

Frequently, you may want to write a program with certain portions of it that can be turned on or turned off. That is to say, when they are turned on, these portions of the program are assembled. If they are turned off, they are not assembled during that particular assembly. ASM contains three pseudos to aid in conditional assembly. They are:

IF ELSE and ENDIF

IF

The IF pseudo conditionally disables assembly of any statements following the IF pseudo operator. The form of the IF pseudo operator is:

IF iexp

If the expression (iexp) evaluates to zero, the statements following the IF pseudo are assembled. If the expression does not evaluate to zero (either negative or positive), any statements in the assembly source code following this expression are skipped until one of the three following pseudos are encountered. The ELSE, ENDIF and END pseudos are not skipped regardless of the value of the expression "iexp".

ELSE

The ELSE pseudo toggles the state of the assembly conditions. The ELSE pseudo is of the form:

ELSE

If the conditional assembly flag is set to skip assembling source code, it is changed so source code is now assembled. If lines of source code prior to encountering the ELSE pseudo are being assembled, those following the ELSE pseudo are skipped until an ELSE, ENDIF, or END is encountered. NOTE: The ELSE segment must appear after an IF statement, but before the associated ENDIF statement.

ENDIF

The ENDIF statement indicates the end of a block of source code designated for conditional assembly. The form of the ENDIF pseudo is:

```
ENDIF
```

Assembly resumes regardless of the current assembly state (assembling or skipping) when the ENDIF conditional assembly pseudo occurs.

End Program, END

The END pseudo indicates the END of a program. The END pseudo takes the form:

```
END iexp
```

where iexp is the program entry point. The program entry point is the memory address where program execution begins. If the END statement is missing, the assembler generates one. If iexp is missing, an error is flagged and ASM uses 042 200A.

Define Label, EQU

The Equate statement is used to assign an arbitrary value to a symbol. The form of the equate statement is:

```
LABEL EQU iexp
```

The equate statement is unique, as it must evaluate on pass one. For this reason, any symbols used within the expression “iexp” must be defined before the assembler encounters the EQU statements. The label is assigned the value of the integer expression “iexp”. This label may not be redefined by subsequent use as a label in any other statement. For example,

```
START EQU *
```

The label START is set equal to the value of the memory location counter, or

```
START EQU 100
```

The label START is set equal to 100.

NOTE: If you omit the label, an error is generated.

Origin Statement, ORG

The Origin statement (ORG) sets the initial value of the memory location counter. The form of the origin statement is:

```
LABEL ORG iexp
```

The expression *iexp* must evaluate on pass one. Therefore, any symbols used within this expression must be defined before the assembler encounters this statement. When the assembler encounters the ORG statement, the memory location counter is set to the expression value. All subsequent object code generated by the assembler is placed in sequential memory locations, starting at the address given by the expression. It is legal to establish a new origin, either before or after a previous origin. If a label is present, it is given the value *iexp*. For example:

```
BEGIN    ORG    42200 A
```

The program is started at location 042 200 (offset octal) and the label BEGIN is assigned the offset octal value 040 200. This is the lowest address the user (programmer) should use.

```
BEGIN    ORG    START+256
```

The memory location counter is set to the previously defined value of the label START + 256. The label BEGIN also assumes this value.

Set Statement, SET

The SET statement assigns an arbitrary value to a desired symbol. The form of the SET statement is:

```
LABEL    SET    iexp
```

The SET pseudo op differs from the EQU pseudo op in that any label defined in a SET statement can be redefined in a following SET statement as many times as desired in the course of the program. The expression “*iexp*” must evaluate during pass one. Therefore, any symbols used within the expression “*iexp*” must be previously defined.

Xtext Statement, XTEXT

The XTEXT statement is used to include the contents of another file in the assembly. The form of the XTEXT statement is:

```
XTEXT    <fname>
```

When the assembler encounters the XTEXT pseudo operation, it locates the specified file <fname>. <fname> must reside upon a disk device and should contain assembly language statements. Note that it may not contain an END statement, nor another XTEXT statement. The statements in <fname> are assembled into the program where the XTEXT statement was encountered. The XTEXT statement itself is normally listed, but the included statements from <fname> normally are not. The C listing control option is provided to cause them to be listed (see LON and LOF pseudo operations).

The file specification <fname> may specify a device code and an extension. If no extension is specified, ASM assumes an extension of ACM. The only device codes which may be specified are SY0: and SY1:. You can only specify "SY1:" if you have a second drive installed on your system. If no device is specified, ASM uses the same device that the main source program resides on. If the named file is not found there, then ASM will try device SY0:. If the named file still cannot be found, then ASM will flag the XTEXT statement with a 'U' error.

The XTEXT statement is normally used to include files containing symbol definitions and commonly used subroutines. For example, Heath provides a file intended to be used with XTEXT, "HDOS.ACM." HDOS.ACM contains symbolic definitions for various operating system function requests. For example, the symbol .EXIT is defined to have the value of 0 (zero). A program including the file HDOS.ACM can use this symbol in generating system requests. This is not only self-documenting, but should a future system revision change the system function codes, the programmer can convert over by simply changing the definitions in HDOS.ACM and reassembling all of his programs, since they all make use of the same definition file, HDOS.ACM.

You can also use XTEXT to include commonly used assembly language subroutines into a program. In this way, a programmer can avoid having to rewrite and redebug the same subroutine for each of his programs. An assembly language programmer will soon build an extensive library of utility subroutines, ready to be XTEXTed into any assembly language program.

Listing Control

ASM provides a number of pseudo operators which affect the listing mode. They control paging, pagination, titles, and subtitles. The listing control pseudos are used to affect easily read documentation; they do not appear in the program listing.

TITLE

The pseudo operator TITLE causes a new page title to be used. The form of the title pseudo op is:

```
TITLE    'new title'
```

Unless the assembler is already at the top of a page, a new page of the assembly listing is generated. This page is given the title contained in the string 'new title'.

STL

The subtitle pseudo (STL) causes a new page subtitle to be set. The form of the subtitle pseudo is:

```
STL      'new subtitle'
```

The subtitle pseudo does not affect pagination. This is to say, it does not generate a new page but simply titles a subsection of the program. Subtitles are frequently used to indicate subroutines or major program modules.

EJECT

The EJECT pseudo causes a new page to be started. The form of the eject pseudo is:

```
EJECT
```

When ASM processes an EJECT pseudo, the output device is instructed to move to the start of a new page during the listing.

SPACE

The space pseudo leaves blank lines in the program listing. The form of the space pseudo is:

```
SPACE    iexp1,iexp2
```


During the assembly listing, iexp1 blank lines are left. If the optional expression iexp2 is specified, the assembler checks during a listing to see if the number of lines remaining on the page is greater than or less than iexp2. If there are less than iexp2 lines remaining on the page, the spacing function is skipped and a new page is started, as if an EJECT pseudo was encountered.

LON (Listing on)

The LON pseudo operator is used to turn-on listing options. The form of the LON pseudo is:

```
LON   CCC
```

Each option is represented by a single character. The characters for the desired options are supplied as CCC. The options and their default modes (if they are not specified) are:

L Master listing

If this option is enabled, all program lines are listed. If it is disabled, only lines containing errors are listed.

DEFAULT MODE: All program lines are listed (normally enabled; disable using LOF).

I Lists the IF-skipped lines. When this option is enabled, all lines skipped due to IF statements are listed (although they are not assembled).
DEFAULT MODE: The skip lines are not contained in the listing.

G Lists all generated bytes. When this option is enabled, all generated bytes appear on the listing. If more than three bytes are generated by a statement, new lines are generated in the listing to display these bytes. NOTE: The DB pseudo can produce many bytes when you are encoding a string. These are not normally listed.
DEFAULT MODE: Lists a maximum of the 3-bytes generated in each statement.

C Lists XTEXT-included lines. When this option is enabled, all lines included via the XTEXT pseudo operator are listed.
DEFAULT MODE: XTEXT lines are not listed.

LOF (Listing off)

The LOF pseudo is identical to the LON pseudo except that the selected options are disabled. The form of the LOF pseudo is:

```
LOF    CCC
```

See LON, above, for a description of the control character CCC.

ERRxx

ASM contains four conditional error pseudo operators. These are of the form:

```
ERRZR    iexp
ERRNZ    iexp
ERRPL    iexp
ERRMI    iexp
```

For each of these pseudo operators, the assembler tests the indicated expression. If the expression matches the expressed error condition, an error code is flagged in the listing. The errors associated with each of the conditional error pseudos are:

```
ERRZR    tests for zero expression
ERRNZ    tests for non-zero expression
ERRPL    tests for positive expression
ERRMI    tests for negative expression
```

These pseudo error tests are particularly useful when you make assumptions about the configuration of various program elements or expressions. You can encode these assumptions into ERRxx pseudos. Any change which causes the code to fail generates an error, flagging the programmer during the listing. For example,

```
LXI    H, AREA1
MOV     B, M           (B) = (AREA1)
INX     H
ERRNZ   AREA2-AEA1-1    Assume area 2 follows area 1
MOV     C, M           (C) = (AREA2)
```

If, when the program is assembled, AREA 1 and AREA 2 have been defined differently, an error flag would warn of this mistake.

GENERATING THE ASSEMBLER

Before you can use the assembler, it must first be generated onto your system disk(s). You can do this by simply copying the file ASM.ABS from the system distribution disk. You will probably want to copy over all files with the .ACM (Assembler Common) extension, via *.ACM. The use of these will be discussed later. Copy the files from the distribution disk via ONECOPY or PIP, if you have a multiple-drive system. See the HDOS Manual, for more information.

Using The Assembler

In order to use the assembler, you must prepare a source using a text editor, such as EDIT. To get you started, Heath has prepared some short assembly language programs which are in Appendix A.

When the source program is ready, type ASM in response to the HDOS prompt (>). HDOS interprets this command as RUN SYØ:ASM.ABS. If the assembler is on SY1:, then type RUN△SY1:ASM. In either case, the assembler will type

```
HDOS Assembler Issue #104.00.00
```

```
*
```

Note that the issue number may be different, but an issue will be shown. The “*” is the assembler’s prompt, asking you to enter a command line in the form

The “*” is the assembler’s prompt, asking you to enter a command line in the form

```
<binary fname>,<listing fname>=<source fname>[/SWITCHa.../SWITCHn]
```

The <binary fname> specification tells ASM where to put the generated binary program. The default extension is .ABS. If you do not wish to generate a binary file, omit the file, but not the following comma.

The <listing fname> specification tells ASM where to put the assembly listing. The default extension is .LST. If you specify no listing file, ASM will not generate one. In that case, any program statements that contain errors will be listed on the system console.

The <source fname> specification tells ASM which file contains the assembly language source program. The default extension is .ASM. You must specify this file, it cannot be omitted. The device specified must be a disk (SYØ: or SY1:).

Switches

There are several switches you may specify at the end of the command line. These switches are all optional, and you can combine any number of them. The legal switches are:

`/LARGE`

This switch tells ASM that the program you wish to assemble is large, and it should use all the available memory. Normally, when assembling, ASM speeds itself up by letting the operating system use a portion of RAM. However, if your program is so large that the assembler runs out of RAM, you will have to reassemble using the `/LARGE` switch. This switch causes ASM to use all the available RAM space for itself, with a slightly slower assembly as a result. For systems with only 12K of RAM, ASM will automatically use all of available memory; specifying `/LARGE` will have no effect.

`/ERR`

This switch causes ASM to write all program lines with errors in them to the console. Of course, the lines are also written in the normal fashion to the listing file. If no listing file is specified, error lines will be automatically written to the console regardless of the `/ERR` switch.

`/PAGE:nn`

ASM writes the source listing file formatted into pages, so that the program can be listed neatly on a printer or a hard-copy terminal. The `/PAGE` switch tells the assembler how many lines are to appear on a page. Note that this is not the size of the page itself; you will want to leave several lines to form a gap between the pages. Thus, for the standard page size of 66 lines, a specification of `/PAGE:60` is about right. This is the default value, so only users with non-standard paper size need specify `/PAGE`.

`/FORM:nn`

When the assembler wishes to start a new page for the listing file, it writes an ASCII form feed character into the listing file. This causes an eject to a new page. If your hard copy device will not respond to a form feed in this way, you can use the `/FORM:nn` switch to have the assembler generate the proper number of line feeds to cause the page eject. The “nn” field is the size of a page (or “form”) for your hard copy device. This must be larger than the specified `/PAGE` value (or default).

The standard size for most computer forms is 66 lines per page; thus, `/FORM:66` should be specified. If, for example, you had paper that held 40 lines per page and you wished to print only on the top half of each page, you could specify `/FORM:40/PAGE:20`. This tells ASM that you want to print 20 lines per page, and that each page is 40 lines long. When the `/FORM:nn` switch is specified, the assembler writes the proper number of carriage-return line feeds to the listing file, instead of the form feed character.

`/LON:ccc`

The `/LON` switch is used to override the listing options specified (via the `LON` and `LOF` pseudo instructions) in the assembly language source code. “ccc” represents one or more listing options, discussed in the description of the `LON` pseudo instruction. A listing option selected by the `/LON` switch cannot be deselected by a `LOF` pseudo instruction in the program.

`/LOF:ccc`

The `/LOF` switch is used to override the listing options specified (via the `LOF` and `LOF` pseudo instructions) in the assembly language source code. “ccc” represents one or more listing options, discussed in the description of the ‘`LOF`’ pseudo instruction. A listing option deselected by the `/LOF` switch cannot be selected by a `LON` pseudo instruction in the program.

Command Line Examples

This section shows several example command lines, with a brief discussion of each. These lines all show assemblies of a sample program, DEMO.ASM

```
* DEM0, DEM0=DEM0 Ⓢ
```

This command would cause the file SYØ:DEMO.ASM to be assembled, with the listing file written to SYØ:DEMO.LST, and the binary file written to SYØ:DEMO.ABS. Note that form feed characters will be used to separate the pages of the listing file.

```
* DEM0.XXX, TT:=DEM0.ASM/FORM:66 Ⓢ
```

This command causes the file SYØ:DEMO.ASM to be assembled, with the listing file written directly to the console terminal (device TT:). The binary file will be written to file SYØ:DEMO.XXX. This example assumes that the console terminal is a Decwriter II, without the form-feed option. Thus, the /FORM switch was specified so the assembler would space the paper correctly.

```
* ,LP:=DEM0/LOF:L Ⓢ
```

This command causes the SYØ:DEMO.ASM file to be assembled, with the listing file written directly to the line printer (device LP:). Since no /FORM switch was specified and the /PAGE switch was defaulted to /PAGE:60, the assembler will write pages of 60 lines (or less) to the line printer, separated by form feed characters. The user in this case wanted a listing of just the errors in his program, without listing all the correct statements. His use of the LOF:L switch specified that no lines were to be listed. Since lines containing errors are always listed on the listing file, the result will be a listing on the printer showing only lines with errors.

```
* =DEM0 Ⓢ
```

This final example shows the user assembling the program SYØ:DEMO.ASM, and producing no binary or listing files. This form is useful to check a program for assembly errors since, in the absence of a listing file, all assembly errors are printed on the console. Note that no binary file will be generated.

Errors

All errors detected by the Heath Assembly Language are flagged directly on the listing in the first three columns. One character is flagged for each error detected. If more than one error is detected, the second error character is placed in column 2 and the third error character is placed in column 3.

<u>CHARACTER</u>	<u>ERROR</u>
U	An undefined symbol. The symbol name does not match any symbol in the symbol assignment table. Check for spelling errors or for a completely undefined symbol.
R	Illegal register specified. Two different errors can cause this message. A non-8080 register may have been specified, or the instruction was not meaningful for the register. For example, a register pair instruction which refers to a single register.
D	Label is doubly defined. The symbolic label has been defined twice in the source program.
A	Operand syntax error. The operand expression is improper. For example, it may evaluate to a number >65535, be a divide by zero, or be nonexistent.
V	Value exceeds eight bits. The result of an expression is greater than 255. This error is not flagged if the op-code called for a 16-bit operand such as an LXI instruction.
F	Format error. A pseudo-op requires a label that is not present in the source code. For example, an EQU pseudo-op requires a label. Too many characters in a label.
O	Unrecognized op-code. The op-code in this statement does not belong to the 8080 instruction set, nor does it belong to the ASM pseudo-op instruction code set. Check for spelling errors or for op-codes used from other microprocessor instruction sets.

CHARACTERERROR

P

Error generated by ERRxx pseudo or reference to a doubly defined label. Note the ERRxx pseudos are generated to flag the user when a test expression does not evaluate satisfactorily.

NOTE: If an assembly generates a great number of errors, it is best to return to the Text Editor, correct as many errors as possible, and reassemble. The reassembly will frequently flag additional errors which are then obvious on the second assembly. If the errors are few, you may load the program and debug it using DEBUG. However, this **does not** result in a correct listing.

APPENDIX A

Assembly Language Interface

Introduction

The HDOS operating system offers a powerful and yet simple interface to assembly language programs. This section discusses the fundamental system commands necessary to execute a simple assembly language program. The advanced features and facilities of HDOS will be discussed elsewhere.

HDOS provides what is called the “environment” for an assembly language program. It loads the program into memory, sets up the stack, handles console and disk device I/O, and provides other services for the program. In return, a programmer must always remember that his program is not the only one running in the computer, the HDOS program is also running in the same machine. A programmer must: be careful not to write into memory locations reserved for HDOS, be sure his program does not destroy the program stack by loading the stack pointer; be sure his program does not turn off interrupts via the DI instruction (except for very short periods of time), and so forth.

Finally, it is important that assembly language programs use the support and facilities of HDOS rather than “doing it themselves.” Using HDOS whenever possible serves two functions: first, it makes the program much more useful and flexible. For example, if your program uses the HDOS console driver rather than communicating directly to the console itself (via IN and OUT instructions), your program automatically takes advantage of the features of the HDOS console system (CTRL-S, CTRL-O, RUBOUT, CTRL-U, etc.) without any extra programming effort for you. Later, when Heath issues a new version of HDOS supporting new devices and/or new features, your program will automatically be able to take advantage of any new feature without having to be modified.

The second reason for using HDOS functions is system compatibility. As mentioned above, new releases of HDOS will be made available periodically. These new versions will fix known bugs, support new devices, and contain powerful new features. Programs which properly use HDOS functions will be able to run under the new versions of HDOS after being reassembled. Programs that “do it themselves” may fail to work under new HDOS releases.

Writing Your Program

In order to successfully run your assembly language program under HDOS, you must follow the simple format shown in Figure 1. Your program must start with the three lines:

```
TITLE    "some descriptive title"
XTEXT    HDOS
ORG      USERFWA
```

The TITLE statement causes an appropriate title to be printed on the assembly listing. The title you use is not important as long as it is meaningful to you. The XTEXT statement prepares the assembler for the HDOS commands you will be including in your program. These are discussed later in this section. Finally, the ORG statement tells the assembler to assemble your program into the user memory area.

After these three lines you will write your program. The last line in the program must be

```
END      xxx
```

where xxx is a label in your program. When you run your program (via the RUN command), execution will begin at the label specified in the END statement.

```
TITLE    "some meaningful title"
XTEXT    HDOS
ORG      USERFWA
XXX      (first line of executable code)
          (your program goes here, see Figures 2, 3, and 4 for examples)
END      xxx
```

Figure 1

Required format for assembly language programs.

Assembling Your Program

The first thing you must do to run an assembly language program is assemble it. This process translates the source language statements into the 8080A binary object codes. A sample program, DEMO.ASM is shown in Figure 2, Page 4-67. You should enter this through the editor. Once you have this program as a source file, you can assemble it. In HDOS command mode, type:

```
>RUN△ASM ⑧  
*DEMO,DEMO=DEMO ⑧
```

Note that you must type the underlined characters; HDOS provides the characters shown without underlining. This command tells the assembler that you want to assemble the file SYØ:DEMO.ASM, producing a listing file called SYØ:DEMO.LST and producing a binary file SYØ:DEMO.ABS. It is this binary file that contains the runnable program. If you have a hard copy device, such as a Decwriter, you can copy the file DEMO.LST onto that device for reference during the remainder of this discussion. If you do not have a hard-copy device, you can refer to the listing of the file DEMO.ASM at the back of this section.

Note that the .ASM, .LST, and .ABS extensions are “defaults” provided by ASM. The assembler will use any specified extensions. Since ASM makes use of HDOS facilities for I/O, ASM is also device independent. For example, if you are assembling a program and want to produce the listing output on your “AT:” device, you need not write the listing file to the disk, copy it to “AT:” and then delete it. Instead, type:

```
*DEMO,AT:=DEMO ⑧
```

and have the listing written directly to the “AT:” device.

Executing Your Program

You must specify the starting address, or entry point, of your program in the END statement. Thus, in the program DEMO.ASM, the END statement says that execution is to start at the label ENTRY. When you type:

```
>RUN△DEMO ⑧
```

HDOS will load the program into memory and start executing it at the label ENTRY.

Returning to HDOS

When your program has finished executing, it must return control to HDOS so you can continue to use the operating system. Your program can do an orderly return to HDOS by executing the two instructions:

```
XRA    A
SCALL  .EXIT
```

which will cause control to return to HDOS. The SCALL .EXIT instruction will be the last one your program will execute.

The SCALL is a special HDOS assembler operation that generates a special two-byte call to the HDOS operating system. The symbol .EXIT indicates the particular type of request you want to make. In this case, you are telling HDOS that you are done executing.

Another way to return control to HDOS is to process CTRL-Cs within your program. In your program initialization, set up CTRL-C processing as follows:

```
.
.
.
LXI H,EXIT
MVI A,003
SCALL .CTLC
.
.
.
```

The end of your program will have the exit routine:

```
.
.
.
EXIT XRA A
SCALL .EXIT
```

A CTRL-C entered while your program is running will cause a return to HDOS.

If you have not dismounted or reset your system volume (see Chapter 1) typing CTRL-Z twice will return to HDOS immediately. However, if your program has a bug and cannot respond to CTRL-C or CTRL-Z, you should re-boot the entire system. This will re-initialize the system. You can run your program under DBUG and isolate the problem in a controlled environment.

Memory Usage

HDOS uses memory locations both below and above your program. It is important that HDOS should know how much of the user memory area, starting at 42200A, your program will be using. In order to be as fast as possible, HDOS will use some of the user RAM area (that part directly below the resident HDOS code) for a work area if the running user program is not using it. Thus, if you are not going to use that RAM, HDOS should be informed so it can use the area. If you are going to use that RAM, HDOS should be informed so it will not use the area for itself.

When you type the command

```
>RUN△<fname> Ⓜ
```

HDOS automatically computes the size of your program as it was assembled. This means that your program must not write into any memory location that you did not declare during the assembly with a DB, DW, or DS statement. For example, if your program needs a 500-byte memory area, you should not write your program in the form:

```

      .      .
      .      .
      .      .
WORK  EQU    *          500 BYTE WORK AREA STARTS HERE
      END    ENTRY

```

and then use the 500-bytes starting at the label WORK. In this case, HDOS would think that your program ended at the label WORK, and have no way of knowing that you were going to use 500 more bytes. You should code the program

```

      .      .
      .      .
      .      .
WORK  DS     500        500 BYTE WORK AREA
      END    ENTRY

```

In this case, HDOS will know that you will be using the 500 bytes at WORK because you declared them in the DS statement.

Typing Lines and Characters

HDOS provides two commands for writing to the console terminal. These are .PRINT, and .SCOUT.

.PRINT

The .PRINT SCALL is used to print a line of text on the system console. Before you issue the .PRINT SCALL, you must load the address of the first byte of the line to be printed in the H and L registers. For example,

```

                LXI      H,LINE
                SCALL    .PRINT          PRINT THE MESSAGE
                .
                .
LINE    DB      12Q,'HI THER','E'+200Q

```

would cause the message
HI THERE
to be printed on the system console.

You have probably noticed that the DB statement in the above example contains more than just the character string 'HI THERE'. The first of these additions is the 12Q. This tells the assembler to start the message with the ASCII character 012 (octal). This is the ASCII "New Line" character. Instead of using the ASCII Carriage Return and Line Feed characters, HDOS uses the New Line character. (Note that New Line has the same octal code as Line Feed; since HDOS does not allow Line Feed characters, there is no confusion.) The New Line character causes a new line to be started on the output device. The rationale behind the use of New Line instead of carriage return line feed is beyond the scope of this Manual; suffice it to say that the use of New Line gives HDOS a device-independent way to cause a new line to be started. The carriage return character should not be used; the line feed character will be interpreted as a New Line (since both are represented by 12Q).

The other item to note about the DB statement is the expression "'E'+200Q". The .PRINT command prints the characters whose address is in the H and L registers until it prints a character with the parity (200Q) bit set. This character is the last one printed. Thus, in the example the expression "'E'+200Q" was used to set the high-order bit on the last 'E' in the message so HDOS would stop typing at that point.

.SCOUT

Use the .SCOUT to type a single character on the console device. The character in the A register is printed on the console terminal. For example,

```

                MVI      A,'X'
                SCALL    .SCOUT          PRINT THE CHARACTER 'X'

```

The high-order bit (the parity bit) is ignored by .SCOUT.

Reading From the Console

HDOS provides the .SCIN command for reading characters from the console terminal, and the one command .CONSL to control character echoing, backspace, and erase-line handling.

.SCIN

The .SCIN command is used to read a single character from the console device. If the 8080 “carry” flag is set after the SCALL instruction, it means that no character has been typed yet. If the carry flag is clear, then a character has been read and is in the A register. It does not matter if the carry flag is set or clear when you execute the SCALL .SCIN. For example,

READ	SCALL	.SCIN	READ A CHARACTER, IF ANY
	JC	READ	NO CHARACTER ENTERED, YET
	STA	CHAR	STORE CHARACTER READ IN MEMORY

.CONSL

The .CONSL command is used to set the mode of console input. There are two modes of input: line mode, and character mode.

When you are inputting in line mode, HDOS saves up the typed characters until you type a RETURN. This is done so HDOS can handle RUBOUT (character delete) and CTRL-U (line delete) functions. If HDOS were to give you the characters one by one as they were typed, it wouldn't be able to ‘take them away again’ if CTRL-U were typed. By saving them all up until you hit the RETURN, HDOS can handle and DELETES and CTRL-Us that are typed. For example, if you were to type the four keys Y, E, S, and RETURN while your program was executing the example shown above, it would not receive any characters until you pressed the RETURN. The next four .SCIN commands would each return with one of the characters. The RETURN key gives the 012Q (New Line) character code. Thus, the four values read when you type YES (RETURN) are 131Q (Y), 105Q (E), 123Q (S) and 012Q (RETURN).

Line mode is very useful when you wish to input a line from the console, since HDOS provides the DELETE and CTRL-U functions for you automatically. For programs that need to read each character immediately after it is typed, there is ‘character mode’. Inputting in character mode causes the typed character to be passed to your program immediately. If the user types RUBOUT or DELETE, the RUBOUT code (177Q) is passed to your program. If the user types CTRL-U, the CTRL-U code (025Q) is passed to your program. Character mode is more flexible than line mode, but it requires your program to handle the RUBOUT and CTRL-U keys.

The .CONSL command also allows you to turn character echoing on and off. If echoing is turned on, then each time the user strikes a character it is typed on the console automatically by HDOS. If echoing is turned off, the character is not typed on the console. If you wish the character to be visible, your program must type it itself, via the .SCOUT command.

To use the .CONSL command, code the following lines:

```
XRA      A
MVI      B,xxx          'xxx' = value discussed below
MVI      C,201Q
SCALL    .CONSL
```

where 'xxx' is

```
000Q FOR LINE MODE WITH ECHO
001Q FOR CHARACTER MODE WITH ECHO
200Q FOR LINE MODE WITHOUT ECHO
201Q FOR CHARACTER MODE WITHOUT ECHO
```

The default mode of HDOS console input is "line mode, with echo". You only need to use the SCALL .CONSL command if you wish some other mode of operation. You can change modes of operation as often as you like.

NOTE: The system must be configured to accept tabs in order to run a demonstration program.

See SET command in the HDOS Manual.


```

.....
TITLE   'DEMO.ASM - HEATH HDOS ASSEMBLY LANGUAGE DEMO'
XTEXT   HDOS
ORG      USERFWA

STL      'DOCUMENTATION'
***      DEMO.ASM - HEATH HDOS ASSEMBLY LANGUAGE.
*
*      DEMO IS A SHORT AND SIMPLE PROGRAM USED TO DEMONSTRATE THE HDOS
*      ASSEMBLER, AND THE HDOS OPERATING SYSTEM.
*
*      THIS PROGRAM SIMPLY PRINTS TWO CODED LINES ON THE
*      SYSTEM CONSOLE TERMINAL.
*
ENTRY    LXI      H,MESA          (HL) = ADDRESS OF 1ST MESSAGE
          SCALL    .PRINT          PRINT FIRST MESSAGE
          LXI      H,MESB          (HL) = ADDRESS OF 2ND MESSAGE
          SCALL    .PRINT          PRINT 2ND MESSAGE
*
*      SEND A BELL TO THE TERMINAL
          MVI      A,070          (A) = ASCII BELL
          SCALL    .SCOUT          RING TERMINAL'S BELL
*
*      RETURN CONTROL TO HDOS OPERATING SYSTEM
          XRA      A
          SCALL    .EXIT          EXIT TO OPERATING SYSTEM
*
*      MESSAGES FOR .PRINT SCALL'S
MESA     DB      120,'HI THERE, SPORTS FANS','!'+2000
          DB      120,'YOUR SYSTEM WORKS FINE','!'+2000
          DB      120,'LIST THE BYTES OF THE NEXT MESSAGE'
          DB      120,'!'+2000
          END      ENTRY          START EXECUTING AT 'ENTRY' LABEL

```

Figure 2

DEMO.ASM


```

.....
TITLE 'DEMO2.ASM - CONSOLE READ DEMO, LINE MODE'
XTEXT HDOS
ORG USERFWA
.....
STL 'WRITTEN 01/23/78'
.....
*** DEMO2.ASM - CONSOLE INPUT DEMO, IN LINE MODE.
*
* THIS IS A SIMPLE DEMONSTRATION PROGRAM THAT INPUTS LINES FROM
* THE CONSOLE, AND TYPES THEM BACK AGAIN.
*
* IF THE LAST LINE YOU ENTERED CONTAINED A PERIOD (',') THEN
* DEMO2 EXITS TO HDOS AFTER TYPING THE LINE.
.....
*** TO RUN THIS PROGRAM, TYPE THE FOLLOWING:
* (DO NOT TYPE COMMENTS IN PARENTHESIS)
*
* >RUN ASM
* *DEMO2.IT:=DEMO2 (WRITES LISTING TO CONSOLE)
* >RUN DEMO2
* HI, I'M DEMO2! (DEMO2 TYPES THIS)
* ABCD (YOU TYPE THIS)
* ABCD (DEMO2 TYPES THIS)
* IS ANYONE THERE? (YOU TYPE THIS)
* IS ANYONE THERE? (DEMO2 TYPES THIS)
* BYE BYE. (YOU TYPE THIS)
* BYE BYE. (DEMO2 TYPES THIS)
* > (DEMO2 EXITS TO THE OPERATING SYSTEM)
.....
STL 'MAIN PROGRAM'
EJECT START A NEW PAGE
ENTRY LXI H,DEMOA EXECUTION STARTS HERE
SCALL PRINT PRINT 'HI!' MESSAGE
*
* LOOP ECHOING LINES
.....
ECHO SCALL SCIN NO CHARACTER YET
JC ECHO
CPI ','
JNE ECHO1 NOT PERIOD CHARACTER
STA ENDFLAG MAKE ENDFLAG NON-ZERO (A ',', IN FACT)
ECHO1 SCALL SCOUT TYPE CHARACTER BACK
LDA ENDFLAG
ANA A
JZ ECHO STILL MORE TO GO
*
* HAVE SEEN ',', WILL RETURN TO HDOS
.....
XRA A
SCALL EXIT RETURN TO HDOS
.....
DEMOA DB 120, 'HI, I'M DEMO2!', 2120
ENDFLAG DB 0 <=0 IF TO EXIT
END ENTRY
.....

```

Figure 4

DEMO2.ASM

Note that although this program appears to echo each character after it is typed, actually it echoes each line after the RETURN has been typed. This is because the program reads characters in line mode. HDOS holds the characters until you press the RETURN key, and then supplies them to the DEMO2 program. Thus, each line typed to this program appears twice: once when HDOS echoed it as it was being typed, and once when DEMO2.ASM types it.


```

.....
TITLE      DEMO3.ASM - CONSOLE READ DEMO, CHARACTER MODE
XTEXT      HDOS
ORG         USERFWA
.....
STL         'WRITTEN 01/23/78'
.....
***        DEMO3.ASM - CONSOLE INPUT DEMO, IN CHARACTER MODE.
*
*          THIS IS A SIMPLE DEMONSTRATION PROGRAM THAT INPUTS CHARACTERS FROM
*          THE CONSOLE, AND TYPES THEM BACK AGAIN.
*
*          IF THE LAST CHARACTER YOU ENTERED CONTAINED A PERIOD (',') THEN
*          DEMO3 EXITS TO HDOS AFTER TYPING THE CHARACTER.
*
.....
***        TO RUN THIS PROGRAM, TYPE THE FOLLOWING:
*          (DO NOT TYPE COMMENTS IN PARENTHESES)
*
*          >RUN ASM
*          *DEMO3,TT:=DEMO3              (WRITES LISTING TO CONSOLE)
*          >RUN DEMO3
*          HI, I'M DEMO3!                (DEMO3 TYPES THIS)
*          AABBCDD                      (YOU TYPE 'ABCD', DEMO3 DUPLICATES IT)
*          XXYY..                        (YOU TYPE 'XY.', DEMO3 ECHOS IT)
*          >                             (DEMO3 EXITS TO THE OPERATING SYSTEM)
*
STL         'MAIN PROGRAM'
EJECT
ENTRY       LXI      H,DEMOA             START A NEW PAGE
            SCALL    .PRINT              EXECUTION STARTS HERE
            PRINT    'HI!' MESSAGE
.....
*          SETUP CHARACTER MODE. SINCE HDOS WILL ECHO
*          THE CHARACTERS, AND THEN DEMO3 WILL TYPE THEM, CHARACTERS WILL
*          BE DOUBLED ON THE SCREEN AS THEY ARE TYPED.
*
XRA         A
MVI         B,0010                      CHARACTER MODE WITH ECHO
MVI         C,2010
SCALL       .CONSL
.....
*          LOOP ECHOING LINES
ECHO        SCALL    .SCIN
JC          ECHO                         NO CHARACTER YET
CPI         ','
JNE         ECHO1
STA         ENDFLAG                      MAKE ENDFLAG NON-ZERO (A ',', IN FACT)
ECHO1       SCALL    .SCOUT              TYPE CHARACTER BACK
LDA         ENDFLAG
ANA         A
JZ          ECHO                         STILL MORE TO GO
.....
*          HAVE SEEN ','. WILL RETURN TO HDOS
XRA         A
SCALL       .EXIT                        RETURN TO HDOS
.....
DEMOA       DB      120,'HI, I'M DEMO3!';2120
ENDFLAG     DB      0                   <=0 IF TO EXIT
.....
END         ENTRY
.....

```

Figure 5
DEMO3.ASM

Note that this program is identical to DEMO2.ASM, except that this program inputs in character mode rather than line mode. This causes a big difference in the response the program makes when you type input to it. DEMO3.ASM echoes each character immediately after it is typed. This causes each character to be printed twice on the screen, once when HDOS echoed it and once when DEMO3.ASM typed it. As an exercise, modify this program to disable the automatic echoing (done by HDOS).

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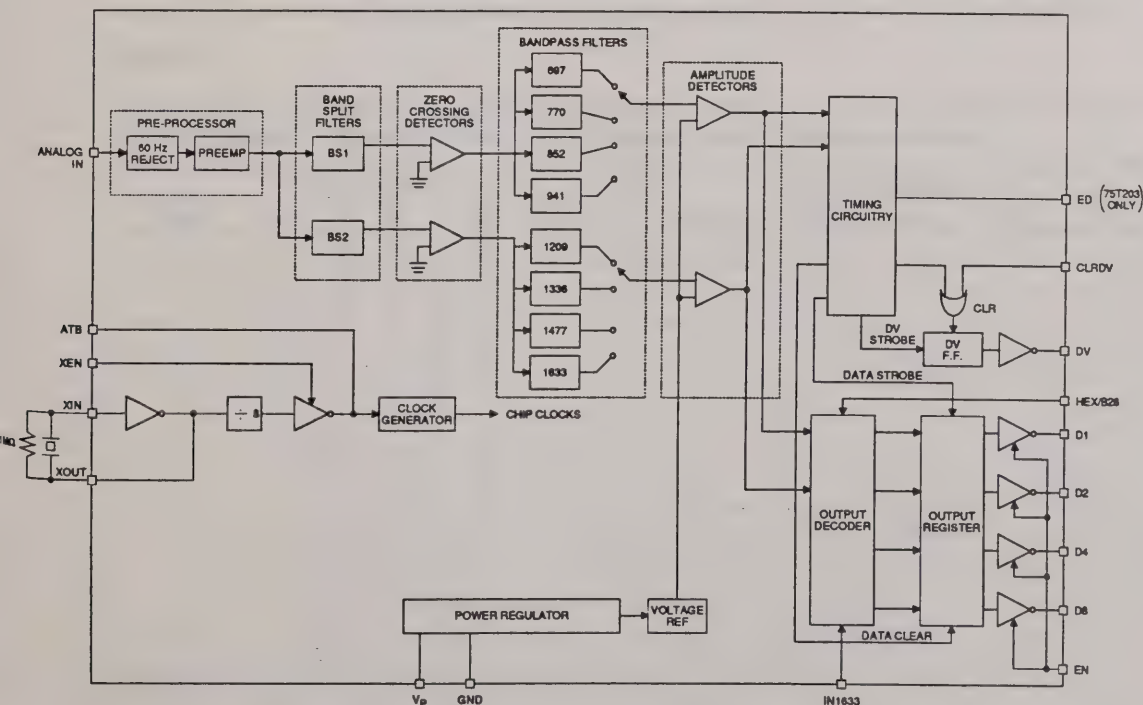
DESCRIPTION

FEATURES

(Continued)

- **Central office quality**
- **NO front-end band-splitting filters required**
- **Single, low-tolerance, 5-volt supply**
- **Detects either 12 or 16 standard DTMF digits**
- **Uses inexpensive 3.579545-MHz crystal for reference**
- **Excellent speech immunity**
- **Output in either 4-bit hexadecimal code or binary coded 2-of-8**
- **18-pin DIP package for high system density**
- **Synchronous or handshake interface**
- **Three-state outputs**
- **Early detect output (SSI 75T203 only)**

BLOCK DIAGRAM



CAUTION: Use handling procedures necessary for a static sensitive component.

Unit 1: Introduction to the Course

The purpose of this unit is to provide a comprehensive overview of the course content and objectives. This section will cover the following topics:

- Course Overview and Objectives
- Unit 1: Introduction to the Course
- Unit 2: Fundamentals of the Subject
- Unit 3: Advanced Topics and Applications
- Unit 4: Research and Analysis
- Unit 5: Final Project and Assessment

Each unit is designed to build upon the previous one, ensuring a solid foundation in the subject matter. The course is structured to provide a balance of theoretical knowledge and practical application, with a focus on developing critical thinking and problem-solving skills.

The following table provides a detailed breakdown of the course structure and the topics covered in each unit.

Unit	Topic	Duration
Unit 1	Introduction to the Course	2 weeks
Unit 2	Fundamentals of the Subject	4 weeks
Unit 3	Advanced Topics and Applications	6 weeks
Unit 4	Research and Analysis	4 weeks
Unit 5	Final Project and Assessment	2 weeks

The course is designed to be completed over a period of 18 weeks, with each unit lasting for a specific duration. The final project and assessment will be completed during the last two weeks of the course.

SSI 75T202/203

5V Low-Power

DTMF Receiver

DESCRIPTION (Continued)

The SSI 75T202 and 75T203 employ state-of-the-art circuit technology to combine digital and analog functions on the same CMOS chip using a standard digital semiconductor process. The analog input is pre-processed by 60-Hz reject and band splitting filters and then hard-limited to provide AGC. Eight bandpass filters detect the individual tones. The digital post-processor times the tone durations and provides the correctly coded digital outputs. Outputs interface directly to standard CMOS circuitry, and are three-state enabled to facilitate bus-oriented architectures.

ANALOG IN

This pin accepts the analog input. It is internally biased so that the input signal may be AC coupled. The input may be DC coupled as long as it does not exceed the positive supply. Proper input coupling is illustrated in Figure 1.

The SSI 75T202 is designed to accept sinusoidal input wave forms but will operate satisfactorily with any input that has the correct fundamental frequency with harmonics less than -20 dB below the fundamental.

CRYSTAL OSCILLATOR

The SSI 75T202 and 75T203 contain an onboard inverter with sufficient gain to provide oscillation when connected to a low-cost television "colorburst" crystal. The crystal oscillator is enabled by tying XEN high. The crystal is connected between XIN and XOUT. A 1 M Ω 10% resistor is also connected between these pins. In this mode, ATB is a clock frequency output. Other SSI 75T202's (or 75T203's) may use the same frequency reference by tying their ATB pins to the ATB of a crystal connected device. XIN and XEN of the auxiliary devices must then be tied high and low respectively. Ten devices may run off a single crystal-connected SSI 75T202 or 75T203 as shown in Figure 2.

HEX/B28

This pin selects the format of the digital output code. When HEX/B28 is tied high, the output is hexadecimal. When tied low, the output is binary coded 2-of-8. The table below describes the two output codes.

Hexadecimal					Binary Coded 2-of-8				
Digit	D8	D4	D2	D1	Digit	D8	D4	D2	D1
1	0	0	0	1	1	0	0	0	0
2	0	0	1	0	2	0	0	0	1
3	0	0	1	1	3	0	0	1	0
4	0	1	0	0	4	0	1	0	0
5	0	1	0	1	5	0	1	0	1
6	0	1	1	0	6	0	1	1	0
7	0	1	1	1	7	1	0	0	0
8	1	0	0	0	8	1	0	0	1
9	1	0	0	1	9	1	0	1	0
0	1	0	1	0	0	1	1	0	1
*	1	0	1	1	*	1	1	0	0
#	1	1	0	0	#	1	1	1	0
A	1	1	0	1	A	0	0	1	1
B	1	1	1	0	B	0	1	1	1
C	1	1	1	1	C	1	0	1	1
D	0	0	0	0	D	1	1	1	1

TABLE 1: OUTPUT CODES

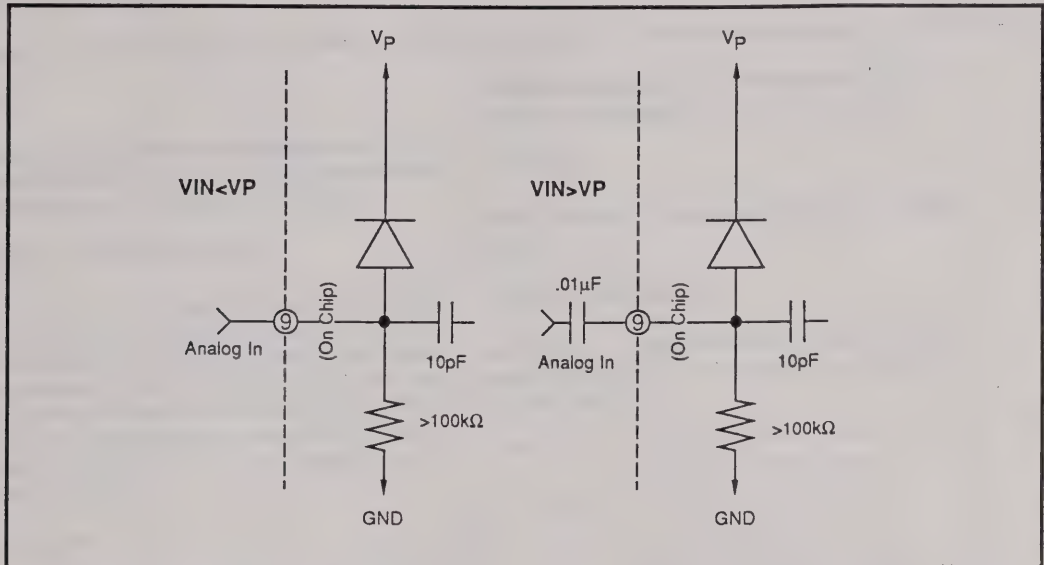


FIGURE 1: INPUT COUPLING

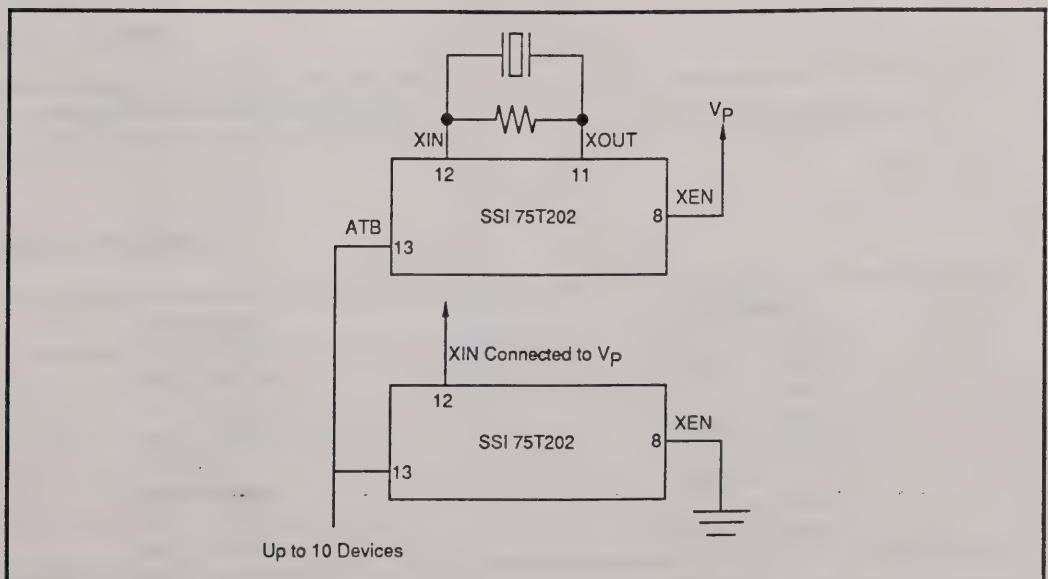


FIGURE 2: CRYSTAL CONNECTIONS

SSI 75T202/203

5V Low-Power

DTMF Receiver

IN1633

When tied high, this pin inhibits detection of tone pairs containing the 1633Hz component. For detection of all 16 standard digits, IN1633 must be tied low.

OUTPUTS D1, D2, D4, D8 and EN

Outputs D1, D2, D4, D8 are CMOS push-pull when enabled (EN high) and open circuited (high impedance) when disabled by pulling EN low. These digital outputs provide the code corresponding to the detected digit in the format programmed by the HEX/B28 pin. The digital outputs become valid after a tone pair has been detected and they are then cleared when a valid pause is timed.

DV and CLRDV

DV signals a detection by going high after a valid tone pair is sensed and decoded at the output pins D1, D2, D4, and D8. DV remains high until a valid pause occurs or the CLRDV is raised high, whichever is earlier.

ED (SSI 75T203 only)

The ED output goes high as soon as the SSI 75T203 begins to detect a DTMF tone pair and falls when the 75T203 begins to detect a pause. The D1, D2, D4, and

D8 outputs are guaranteed to be valid when DV is high, but are not necessarily valid when ED is high.

N/C PINS

These pins have no internal connection and may be left floating.

DTMF DIALING MATRIX

See Figure 3. Please make note that column 3 is for special applications and is not normally used in telephone dialing.

	Col 0	Col 1	Col 2	Col 3
Row 0	1	2	3	A
Row 1	4	5	6	B
Row 2	7	8	9	C
Row 3	*	0	#	D

FIGURE 3: DTMF DIALING MATRIX

DETECTION FREQUENCY

Low Group f_0	High Group f_0
Row 0 = 697 Hz	Column 0 = 1209 Hz
Row 1 = 770 Hz	Column 1 = 1336 Hz
Row 2 = 852 Hz	Column 2 = 1477 Hz
Row 3 = 941 Hz	Column 3 = 1633 Hz

SSI 75T202/203

5V Low-Power

DTMF Receiver

ABSOLUTE MAXIMUM RATINGS

(Operation above absolute maximum ratings may damage the device. All SSI 75T202/203 unused inputs must be connected to V_P or GND, as appropriate.)

PARAMETER	CONDITIONS	RATING
DC Supply Voltage - V_P		+7V
Operating Temperature		-40°C to +85°C Ambient
Storage Temperature		-65°C to +150°C
Power Dissipation (25°C)		65mW
Input Voltage	All inputs except ANALOG IN	($V_P + .5V$) to $-.5V$
ANALOG IN Voltage		($V_P + .5V$) to ($V_P - 10V$)
DC Current into any Input		$\pm 1.0mA$
Lead Temperature	Soldering, 10 sec.	300°C

ELECTRICAL CHARACTERISTICS

(-40°C $\leq T_A \leq$ +85°C, $V_P = 5V \pm 10\%$)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Frequency Detect Bandwidth		$\pm(1.5+2Hz)$	± 2.3	± 3.5	% of f_0
Amplitude for Detection	each tone	-32		-2	dBm ref. to 600 Ω
Minimum Acceptable Twist	$Twist = \frac{High\ Tone}{Low\ Tone}$	-10		+10	dB
60-Hz Tolerance				0.8	Vrms
Dial Tone Tolerance	"precise" dial tone			0dB	dB*
Talk Off	MITEL tape #CM 7290		2		hits
Digital Outputs (except XOUT)	"0" level, 400 μA load	0		0.5	V
	"1" level, 200 μA load	$V_P - 0.5$		V_P	V
Digital Inputs	"0" level	0		0.3 V_P	V
	"1" level	0.7 V_P		V_P	V
Power Supply Noise	wide band			10	mV p-p
Supply Current	$T_A = 25^\circ C$		10	16	mA
Noise Tolerance	MITEL tape #CM 7290			-12	dB*
Input Impedance	$V_P \geq V_{IN} \geq V_P - 10$	100K Ω 15pF			
* dB referenced to lowest amplitude tone					



SSI 75T202/203

5V Low-Power

DTMF Receiver

SSI 75T202/203 TIMING

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNITS
t _{ON} Tone Time	for detection	40	-	-	ms
	for rejection	-	-	20	ms
t _{OFF} Pause Time	for detection	40	-	-	ms
	for rejection	-	-	20	ms
t _D Detect Time		25	-	46	ms
t _R Release Time		35	-	50	ms
t _{SU} Data Setup Time		7	-	-	μs
t _H Data Hold Time		4.2	-	5.0	ms
t _{CL} DV Clear Time		-	160	250	ns
t _{PW} CLRDV Pulse Width		200	-	-	ns
t _{ED} ED Detect Time		7	-	22	ms
t _{ER} ED Release Time		2	-	18	ms
Output Enable Time	C _L = 50pF, R _L = 1KΩ	-	-	200	ns
Output Disable Time	C _L = 35pF, R _L = 500Ω	-	-	200	ns
Output Rise Time	C _L = 50pF	-	-	200	ns
Output Fall Time	C _L = 50pF	-	160	200	ns

SSI 75T202/203 TIMING (Continued)

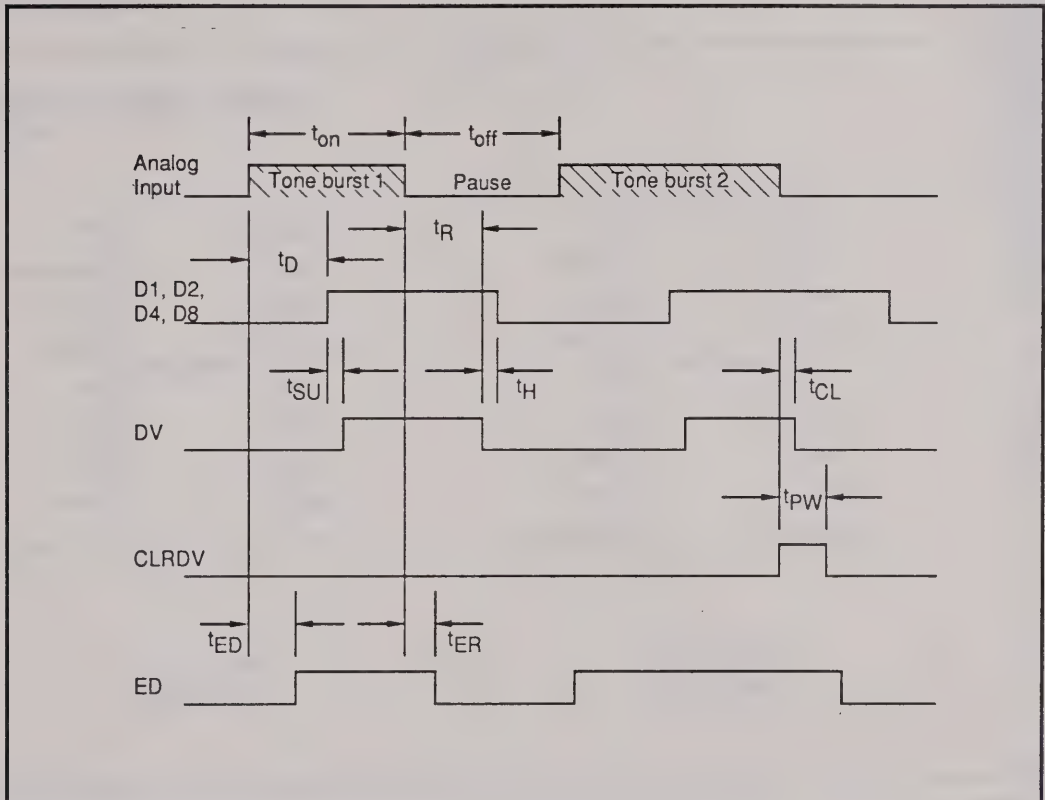


FIGURE 4: TIMING DIAGRAM

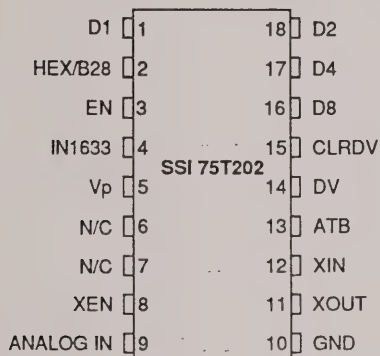


SSI 75T202/203

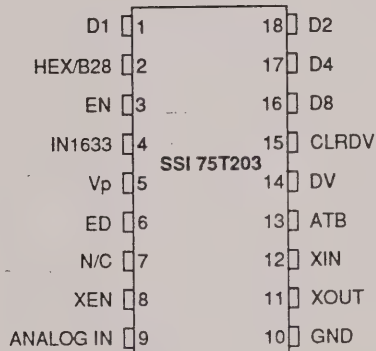
5V Low-Power

DTMF Receiver

PACKAGE PIN DESIGNATIONS (TOP VIEW)



18 - Pin DIP
SSI 75T202



18 - Pin DIP
SSI 75T203

ORDERING INFORMATION

PART DESCRIPTION	ORDER NO.	PKG. MARK
SSI 75T202 18-pin Plastic DIP	SSI 75T202-IP	75T202-IP
SSI 75T203 18-pin Plastic DIP	SSI 75T203-IP	75T203-IP

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COS/MOS 8-Stage Shift-and-Store Bus Register

High-Voltage Types (20-Volt Rating)

The RCA-CD4094B is an 8-stage serial shift register having a storage latch associated with each stage for strobing data from the serial input to parallel buffered 3-state outputs. The parallel outputs may be connected directly to common bus lines. Data is shifted on positive clock transitions. The data in each shift register stage is transferred to the storage register when the STROBE input is high. Data in the storage register appears at the outputs whenever the OUTPUT-ENABLE signal is high.

Two serial outputs are available for cascading a number of CD4094B devices. Data is available at the Q_S serial output terminal on positive clock edges to allow for high-speed operation in cascaded systems in which the clock rise time is fast. The same serial information, available at the Q_S terminal on the next negative clock edge, provides a means for cascading CD4094B devices when the clock rise time is slow.

The CD4094B types are supplied in 16-lead hermetic dual-in-line ceramic packages (D and F suffixes), 16-lead dual-in-line plastic package (E suffix), 16-lead ceramic flat package (K suffix), and in chip form (H suffix).

Features:

- 3-state parallel outputs for connection to common bus
- Separate serial outputs synchronous to both positive and negative clock edges for cascading
- Medium speed operation — 5 MHz at 10 V (typ.)
- Standardized, symmetrical output characteristics
- 100% tested for quiescent current at 20 V
- Maximum input current of 1 μ A at 18 V over full package-temperature range; 100 nA at 18 V and 25°C
- Noise margin (full package temperature range):
1 V at V_{DD} = 5 V 2 V at V_{DD} = 10 V
2.5 V at V_{DD} = 15 V
- 5-V, 10-V, and 15-V parametric ratings
- Meets all requirements of JEDEC Tentative Standard No. 13A, "Standard Specifications for Description of 'B' Series CMOS Devices"

Applications:

- Serial-to-parallel data conversion
- Remote control holding register
- Dual-rank shift, hold, and bus applications

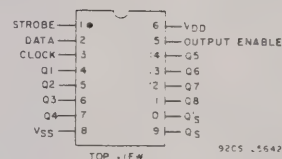
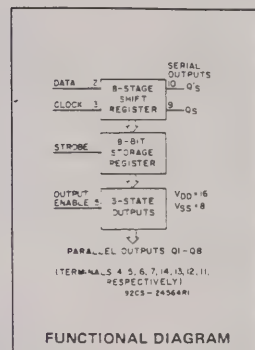


Fig. 1 — Terminal assignment.

MAXIMUM RATINGS, Absolute-Maximum Values:

DC SUPPLY-VOLTAGE RANGE, (V _{DD})	-0.5 to +20 V
(Voltages referenced to V _{SS} Terminal)	
INPUT VOLTAGE RANGE, ALL INPUTS	-0.5 to V _{DD} +0.5 V
DC INPUT CURRENT, ANY ONE INPUT	±10 mA
POWER DISSIPATION PER PACKAGE (P _D):	
For T _A = -40 to +60°C (PACKAGE TYPE E)	500 mW
For T _A = +60 to +85°C (PACKAGE TYPE E)	Derate Linearly at 12 mW/°C to 200 mW
For T _A = -55 to +100°C (PACKAGE TYPES D, F, K)	500 mW
For T _A = +100 to +125°C (PACKAGE TYPES D, F, K)	Derate Linearly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR	
FOR T _A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types)	100 mW
OPERATING-TEMPERATURE RANGE (T _A):	
PACKAGE TYPES D, F, K, H	-55 to +125°C
PACKAGE TYPE E	-40 to +85°C
STORAGE TEMPERATURE RANGE (T _{stg})	-65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):	
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max.	+265°C

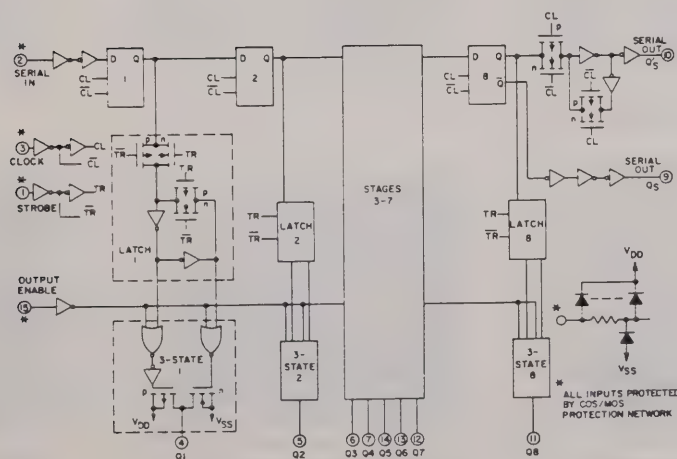


Fig. 2 — CD4094B Logic diagram.

TRUTH TABLE									
CL*	Output Enable	Strobe	Data	Parallel Outputs		Serial Outputs			
				Q1	Q2	Q5*	Q6*	Q7	Q8
0	0	X	X	OC	OC	NC	NC	Q7	NC
0	X	X	X	OC	OC	NC	NC	Q7	NC
1	0	X	X	NC	NC	Q7	NC	Q7	NC
1	1	0	0	0	0	Q5	Q6	Q7	NC
1	1	1	1	1	1	Q5	Q6	Q7	NC
1	1	1	1	NC	NC	NC	NC	Q7	Q8

- * = Level Change
X = Don't Care
NC = No Change
OC = Open Circuit
- Logic 1 ≡ High
Logic 0 ≡ Low
- * At the positive clock edge information in the 7th shift register stage is transferred to the 8th register stage and the Q₈ output

CD 994B Types

RECOMMENDED OPERATING CONDITIONS at $T_A = 25^{\circ}\text{C}$, Except as Noted.
For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	VDD (V)	LIMITS		UNITS
		MIN.	MAX.	
Supply-Voltage Range (For T_A =Full Package-Temperature Range)		3	18	V
Data Setup Time, t_S	5	125	—	ns
	10	55	—	
	15	35	—	
Clock Pulse Width, t_W	5	200	—	ns
	10	100	—	
	15	83	—	
Clock Input Frequency, f_{CL}	5		1.25	MHz
	10	dc	2.5	
	15		3	
Clock Input Rise or Fall time, t_{rCL} , t_{fCL} *	5		15	μs
	10	—	5	
	15		5	
Strobe Pulse Width, t_W	5	200	—	ns
	10	80	—	
	15	70	—	

* If more than one unit is cascaded t_{fCL} (for Q_S only) should be made less than or equal to the sum of the fixed propagation delay at 50 pF and the transition time of the output stage for the estimated capacitive load.

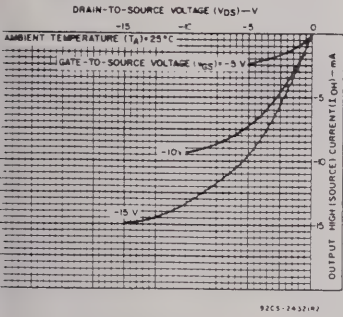


Fig. 5 - Minimum output low (sink) current characteristics.

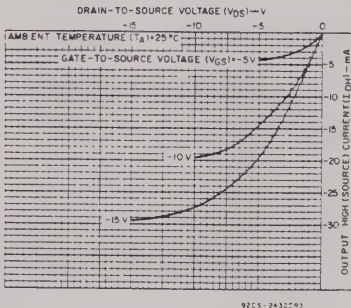


Fig. 6 - Typical output high (source) current characteristics.

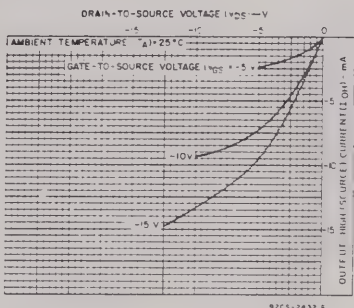


Fig. 7 - Minimum output high (source) current characteristics.

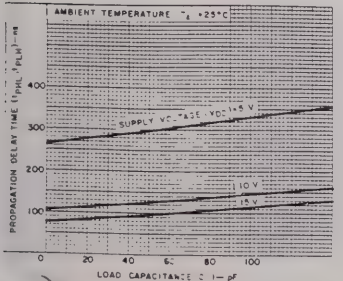


Fig. 8 - Clock-to-serial output Q_S propagation delay vs C_L .

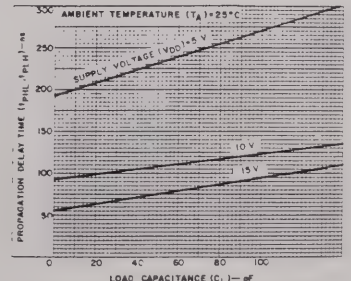


Fig. 9 - Clock-to-parallel output propagation delay vs C_L .

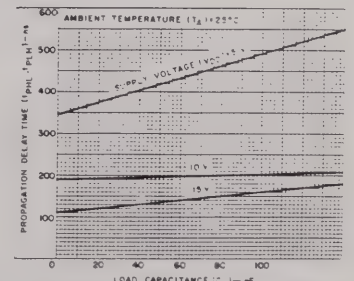


Fig. 10 - Clock-to-parallel output propagation delay vs C_L .

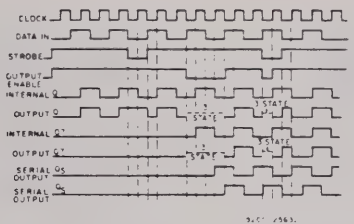


Fig. 3 - Timing diagram.

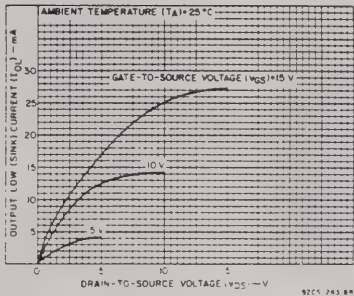


Fig. 4 - Typical output low (sink) current characteristics.

STATIC ELECTRICAL CHARACTERISTICS

CHARACTER- ISTIC	CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C)							UNITS
				Values at -55, +25, +125 Apply to D,K,F,H Packages Values at -40, +25, +85 Apply to E Package							
	V _O (V)	V _{IN} (V)	V _{DD} (V)	+25							
-55				-40	+85	+125	Min.	Typ.	Max.		
Quiescent Device Current, I _{DD} Max.	—	0.5	5	5	5	150	150	—	0.04	5	μA
	—	0.10	10	10	10	300	300	—	0.04	10	
	—	0.15	15	20	20	600	600	—	0.04	20	
	—	0.20	20	100	100	3000	3000	—	0.08	100	
Output Low (Sink) Current I _{OL} Min.	0.4	0.5	5	0.64	0.61	0.42	0.36	0.51	1	—	mA
	0.5	0.10	10	1.6	1.5	1.1	0.9	1.3	2.6	—	
	1.5	0.15	15	4.2	4	2.8	2.4	3.4	6.8	—	
Output High (Source) Current, I _{OH} Min.	4.6	0.5	5	-0.64	-0.61	-0.42	-0.36	-0.51	-1	—	mA
	2.5	0.5	5	-2	-1.8	-1.3	-1.15	-1.6	-3.2	—	
	9.5	0.10	10	-1.6	-1.5	-1.1	-0.9	-1.3	-2.6	—	
	13.5	0.15	15	-4.2	-4	-2.8	-2.4	-3.4	-6.8	—	
Output Voltage: Low-Level, V _{OL} Max.	—	0.5	5	0.05			—		0	0.05	V
	—	0.10	10	0.05			—		0	0.05	
	—	0.15	15	0.05			—		0	0.05	
Output Voltage: High-Level, V _{OH} Min.	—	0.5	5	4.95			4.95		5	—	V
	—	0.10	10	9.95			9.95		10	—	
	—	0.15	15	14.95			14.95		15	—	
Input Low Voltage, V _{IL} Max.	0.5, 4.5	—	5	1.5			—		—	1.5	V
	1.9	—	10	3			—		—	3	
	1.5, 13.5	—	15	4			—		—	4	
Input High Voltage, V _{IH} Min.	0.5, 4.5	—	5	3.5			3.5		—	—	V
	1.9	—	10	7			7		—	—	
	1.5, 13.5	—	15	11			11		—	—	
Input Current I _{IN} Max.	—	0.18	18	±0.1	±0.1	±1	±1	—	±10 ⁻⁵	±0.1	μA
3-State Output Leakage Current I _{OUT} Max	0.18	0.18	18	±0.4	±0.4	±12	±12		±10 ⁻⁴	±0.4	μA

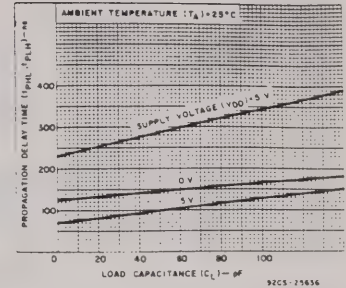


Fig. 11 - Strobe-to-parallel output propagation delay vs C_L .

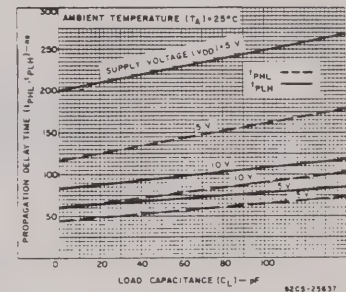


Fig. 12 - Output enable-to-parallel output propagation delay vs C_L .

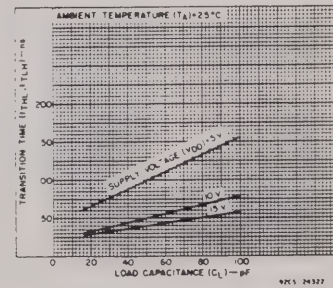


Fig. 13 - Typical transition time vs. load capacitance

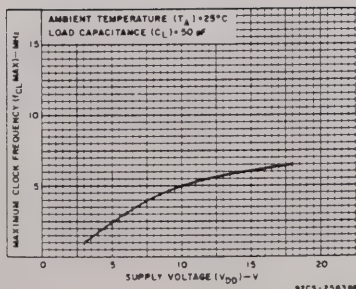


Fig. 14 - Typical maximum-clock-frequency vs. supply voltage.

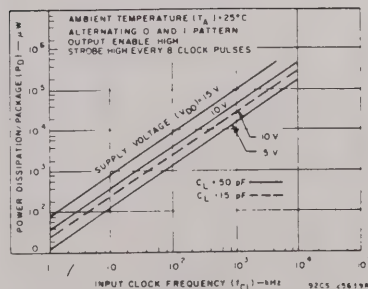


Fig. 15 - Dynamic power dissipation vs input clock frequency.

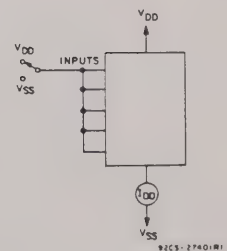


Fig. 16 - Quiescent device current test circuit.

CD4094B Types

DYNAMIC ELECTRICAL CHARACTERISTICS

At $T_A=25^\circ\text{C}$; Input $t_r, t_f = 20\text{ ns}$, $C_L = 50\text{ pF}$, $R_L = 200\text{ k}\Omega$

CHARACTERISTIC	VDD (V)	LIMITS			UNITS
		MIN.	TYP.	MAX.	
Propagation Delay Time, t_{PHL}, t_{PLH}	5	—	300	600	ns
Clock to Serial Output Q_S	10	—	125	250	
	15	—	95	190	
Clock to Serial Output Q'_S	5	—	230	460	ns
	10	—	110	220	
	15	—	75	150	
Clock to Parallel Output	5	—	420	840	ns
	10	—	195	390	
	15	—	135	270	
Strobe to Parallel Output	5	—	290	580	ns
	10	—	145	290	
	15	—	100	200	
Output Enable to Parallel Output: High-to-Low, t_{PHL}	5	—	140	280	ns
	10	—	75	150	
	15	—	55	110	
Low-to-High, t_{PLH}	5	—	225	450	ns
	10	—	95	190	
	15	—	70	140	
Minimum Strobe Pulse Width, t_W	5	—	100	200	ns
	10	—	40	80	
	15	—	35	70	
Minimum Clock Pulse Width, t_W	5	—	100	200	ns
	10	—	50	100	
	15	—	40	83	
Minimum Data Setup Time, t_S	5	—	60	125	ns
	10	—	30	55	
	15	—	20	35	
Transition Time; t_{THL}, t_{TLH}	5	—	100	200	ns
	10	—	50	100	
	15	—	40	80	
Maximum Clock Input Rise or Fall Time, t_{rCL}, t_{fCL}	5	15	—	—	μs
	10	5	—	—	
	15	5	—	—	
Maximum Clock Input Frequency, f_{CL}	5	1.25	2.5	—	MHz
	10	2.5	5	—	
	15	3	6	—	
Input Capacitance C_{IN} (Any Input)	—	—	5	7.5	pF

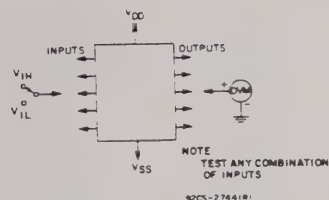


Fig. 17 - Input voltage test circuit.

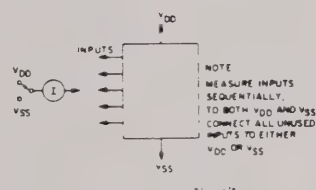


Fig. 18 - Input current test circuit.

TYPICAL APPLICATION

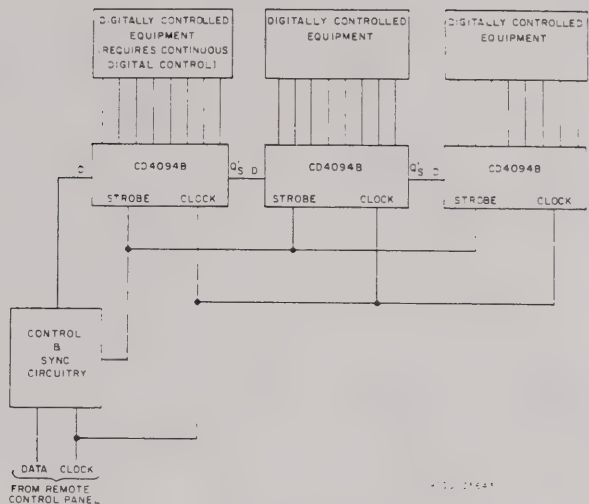
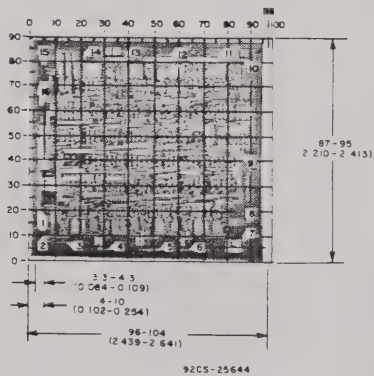


Fig. 19 — Remote control holding register.

Dimensions and Pad Layout for CD4094B Chip.

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

The photographs and dimensions of each COS/MOS chip represent a chip when it is part of the wafer. When the wafer is cut into chips, the cleavage angles are 57° instead of 90° with respect to the face of the chip. Therefore, the isolated chip is actually 7 mils (0.17 mm) larger in both dimensions.



CD4098B Types

CMOS/MOS Dual Monostable Multivibrator

High-Voltage Types (20-Volt Rating)

The RCA-CD4098B dual monostable multivibrator provides stable retriggerable/resettable one-shot operation for any fixed-voltage timing application.

An external resistor (R_X) and an external capacitor (C_X) control the timing for the circuit. Adjustment of R_X and C_X provides a wide range of output pulse widths from the Q and \bar{Q} terminals. The time delay from trigger input to output transition (trigger propagation delay) and the time delay from reset input to output transition (reset propagation delay) are independent of R_X and C_X .

Leading-edge-triggering (+TR) and trailing-edge-triggering (-TR) inputs are provided or triggering from either edge of an input pulse. An unused +TR input should be tied to V_{SS} . An unused -TR input should be tied to V_{DD} . A RESET (on low level) is provided or immediate termination of the output pulse or to prevent output pulses when power is turned on. An unused RESET input should be tied to V_{DD} . However, if an entire section of the CD4098B is not used, its RESET should be tied to V_{SS} . See Table I.

In normal operation the circuit triggers (except the output pulse one period) on the appearance of each new trigger pulse. For operation in the non-retriggerable mode, \bar{Q} is connected to -TR when leading-edge triggering (+TR) is used or Q is connected to +TR when trailing-edge triggering (-TR) is used.

The time period (T) for this multivibrator can be approximated by: $T_X = \frac{1}{2} R_X C_X$ for $C_X \gg 0.01 \mu F$. Time periods as a function of R_X for values of C_X and V_{DD} are given in Fig. 8. Values of T vary from unit to unit and as a function of voltage, temperature, and $R_X C_X$.

The minimum value of external resistance, R_X , is 5 k Ω . The maximum value of external capacitance, C_X , is 100 μF . Fig. 9 shows time periods as a function of C_X for values of R_X and V_{DD} .

The output pulse width has variations of $\pm 2.5\%$ typically, over the temperature range of $-55^\circ C$ to $125^\circ C$ for $C_X = 1000$ pF and $R_X = 100$ k Ω .

For power supply variations of $\pm 5\%$, the output pulse width has variations of $\pm 0.5\%$ typically, for $V_{DD} = 10$ V and 15 V and $\pm 1\%$ typically, for $V_{DD} = 5$ V at $C_X = 1000$ pF and $R_X = 5$ k Ω .

The CD4098B types are supplied in 16-lead hermetic dual-in-line ceramic packages (D and E suffixes), 16-lead dual-in-line plastic packages (K suffix), 16-lead ceramic flat packages (S suffix), and in chip form (H suffix).

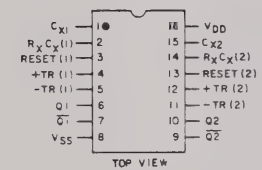
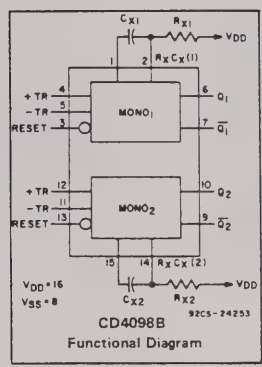
The CD4098B is similar to type MC14528.

Features:

- Retriggerable/resettable capability
- Trigger and reset propagation delays independent of R_X , C_X
- Triggering from leading or trailing edge
- Q and \bar{Q} buffered outputs available
- Separate resets
- Wide range of output-pulse widths
- 100% tested for maximum quiescent current at 20 V
- Maximum input current of 1 μA at 18 V over full package-temperature range; 100 nA at 18 V and $25^\circ C$
- Noise margin (full package-temperature range):
 - 1 V at $V_{DD} = 5$ V
 - 2 V at $V_{DD} = 10$ V
 - 2.5 V at $V_{DD} = 15$ V
- 5-V, 10-V, and 15-V parametric ratings
- Standardized, symmetrical output characteristics
- Meets all requirements of JEDEC Tentative Standard No. 13A, "Standard Specifications for Description of 'B' Series CMOS Devices."

Applications:

- Pulse delay and timing
- Pulse shaping
- Astable multivibrator



TERMINALS 1, 8, 15 ARE ELECTRICALLY CONNECTED INTERNALLY

92CS-2484BRI

TERMINAL ASSIGNMENT

MAXIMUM RATINGS, Absolute-Maximum Values

DC SUPPLY-VOLTAGE RANGE, (V_{DD}) (Voltages referenced to V_{SS} Terminal)	-0.5 to +20 V
INPUT VOLTAGE RANGE, ALL INPUTS	-0.5 to $V_{DD} + 0.5$ V
DC INPUT CURRENT, ANY ONE INPUT	± 10 mA
POWER DISSIPATION PER PACKAGE (P_D)	
For $T_A = -40$ to $+60^\circ C$ (PACKAGE TYPE E)	500 mW
For $T_A = +60$ to $+85^\circ C$ (PACKAGE TYPE E)	Derate Linearly at 12 mW/ $^\circ C$ to 200 mW
For $T_A = -55$ to $+100^\circ C$ (PACKAGE TYPES D, F, K)	500 mW
For $T_A = +100$ to $+125^\circ C$ (PACKAGE TYPES D, F, K)	Derate Linearly at 12 mW/ $^\circ C$ to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR	
FOR $T_A =$ FULL PACKAGE-TEMPERATURE RANGE (All Package Types)	100 mW
OPERATING-TEMPERATURE RANGE (T_A)	
PACKAGE TYPES D, F, K, H	-55 to $+125^\circ C$
PACKAGE TYPE E	-40 to $+85^\circ C$
STORAGE TEMPERATURE RANGE (T_{stg})	-65 to $+150^\circ C$
LEAD TEMPERATURE (DURING SOLDERING)	
At distance 1/16 = 1.32 inch (1.59 \pm 0.79 mm) from case for 10 s max	$+265^\circ C$

RECOMMENDED OPERATING CONDITIONS

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	V_{DD} V	LIMITS		UNITS
		MIN.	MAX.	
Supply-Voltage Range (For $T_A =$ Full Package-Temperature Range)	—	3	18	V
Trigger Pulse Width $t_W(TR)$	5 10 15	140 60 40	— — —	ns
Reset Pulse Width $t_W(R)$ (This is a function of C_X)	—	See Dynamic Char. Chart and Fig. 11		—
Trigger Rise or Fall Time $t_r(TR)$, $t_f(TR)$	5 - 15	—	100	μs

TABLE I

CD4098B FUNCTIONAL TERMINAL CONNECTIONS

FUNCTION	V _{DD} TO TERM. NO.		V _{SS} TO TERM. NO.		INPUT PULSE TO TERM. NO.		OTHER CONNECTIONS	
	MONO ₁	MONO ₂	MONO ₁	MONO ₂	MONO ₁	MONO ₂	MONO ₁	MONO ₂
Leading-Edge Trigger/Retriggerable	3, 5	11, 13			4	12		
Leading-Edge Trigger/Non-retriggerable	3	13			4	12	5-7	11-9
Trailing-Edge Trigger/Retriggerable	3	13	4	12	5	11		
Trailing-Edge Trigger/Non-retriggerable	3	13			5	11	4-6	12-10
Unused Section	5	11	3, 4	12, 13				

NOTES:

1. A RETRIGGERABLE ONE-SHOT MULTIVIBRATOR HAS AN OUTPUT PULSE WIDTH WHICH IS EXTENDED ONE FULL TIME PERIOD (T_X) AFTER APPLICATION OF THE LAST TRIGGER PULSE.
2. A NON-RETRIGGERABLE ONE-SHOT MULTIVIBRATOR HAS A TIME PERIOD T_X REFERENCED FROM THE APPLICATION OF THE FIRST TRIGGER PULSE.

INPUT PULSE TRAIN

RETRIGGERABLE MODE PULSE WIDTH (+TR MODE)

NON-RETRIGGERABLE MODE PULSE WIDTH (+TR MODE)

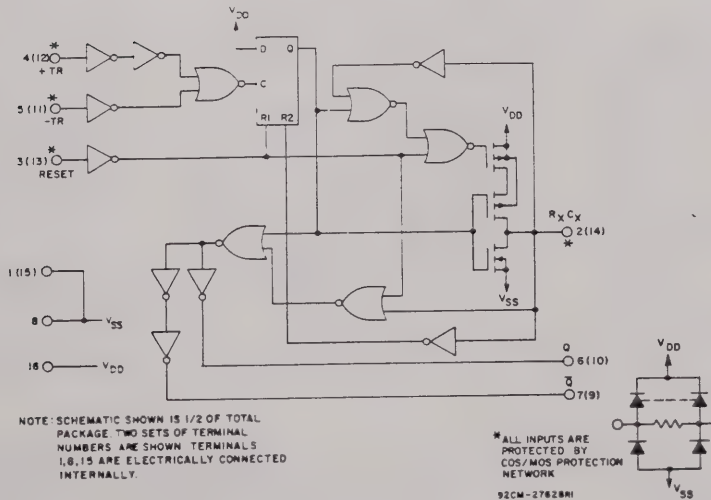
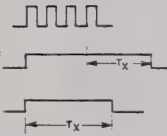


Fig. 4 — CD4098B logic diagram.

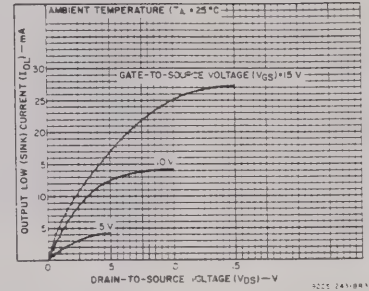


Fig. 1 — Typical output low (sink) current characteristics.

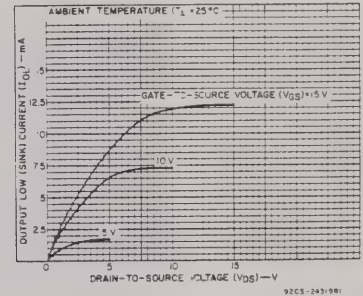


Fig. 2 — Minimum output low (sink) current characteristics.

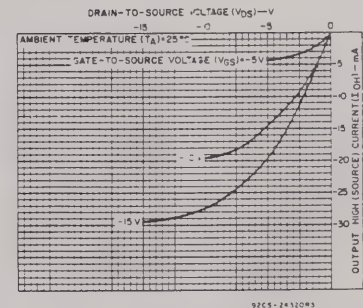


Fig. 3 — Typical output high (source) current characteristics.

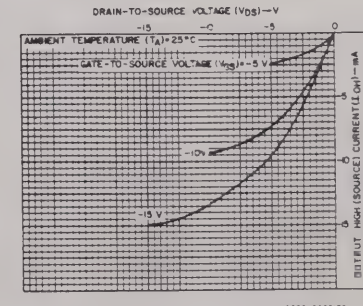


Fig. 5 — Minimum output high (source) current characteristics.

CD4098B Types

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C)								UNITS
				Values at -55,+25,+125 Apply to D,K,F,H Pkgs. Values at -40,+25,+85 Apply to E Pkgs.								
	V _O (V)	V _{IN} (V)	V _{DD} (V)	-55	-40	+85	+125	+25				
								Min.	Typ.	Max.		
Quiescent Device Current I _{DD} Max.	—	0.5	5	1	1	30	30	—	0.02	1	μA	
	—	0.10	10	2	2	60	60	—	0.02	2		
	—	0.15	15	4	4	120	120	—	0.02	4		
	—	0.20	20	20	20	600	600	—	0.04	20		
Output Low (Sink) Current, I _{OL} Min.	0.4	0.5	5	0.64	0.61	0.42	0.36	0.51	1	—	mA	
	0.5	0.10	10	1.6	1.5	1.1	0.9	1.3	2.6	—		
	1.5	0.15	15	4.2	4	2.8	2.4	3.4	6.8	—		
Output High (Source) Current, I _{OH} Min.	4.6	0.5	5	-0.64	-0.61	-0.42	-0.36	-0.51	-1	—	mA	
	2.5	0.5	5	-2	-1.8	-1.3	-1.15	-1.6	-3.2	—		
	9.5	0.10	10	-1.6	-1.5	-1.1	-0.9	-1.3	-2.6	—		
	13.5	0.15	15	-4.2	-4	-2.8	-2.4	-3.4	-6.8	—		
Output Voltage: Low-Level, V _{OL} Max.	—	0.5	5	0.05				—	0	0.05	V	
	—	0.10	10	0.05				—	0	0.05		
	—	0.15	15	0.05				—	0	0.05		
Output Voltage: High-Level, V _{OH} Min.	—	0.5	5	4.95				4.95	5	—	V	
	—	0.10	10	9.95				9.95	10	—		
	—	0.15	15	14.95				14.95	15	—		
Input Low Voltage, V _{IL} Max.	0.5,4.5	—	5	1.5				—	—	1.5	V	
	1.9	—	10	3				—	—	3		
	1.5,13.5	—	15	4				—	—	4		
Input High Voltage, V _{IH} Min.	0.5,4.5	—	5	3.5				3.5	—	—	V	
	1.9	—	10	7				7	—	—		
	1.5,13.5	—	15	11				11	—	—		
Input Current, I _{IN} Max.	—	0.18	18	±0.1	±0.1	±1	±1	—	±10 ⁻⁵	±0.1	μA	

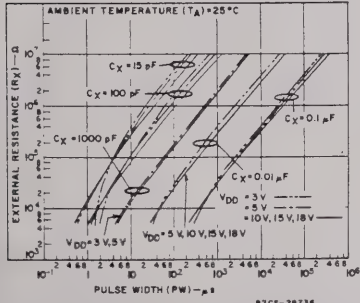


Fig. 8 – Typical external resistance vs. pulse width.

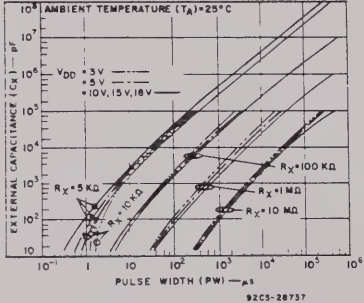


Fig. 9 – Typical external capacitance vs. pulse width.

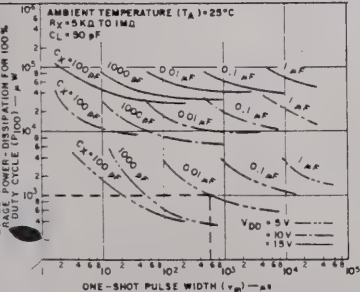


Fig. 11 – Average power dissipation vs. one-shot pulse width.

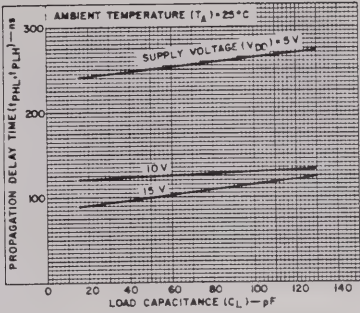


Fig. 6 – Typical propagation delay time vs. load capacitance, trigger into Q out. (All values of CX and RX.)

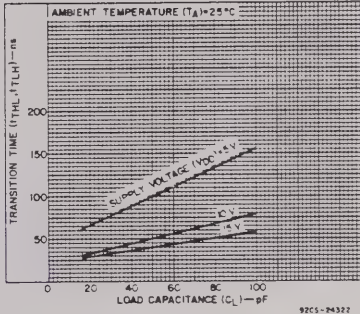


Fig. 7 – Transition time vs. load capacitance for RX = 5 kΩ-10000 kΩ and CX = 15 pF-10000 pF.

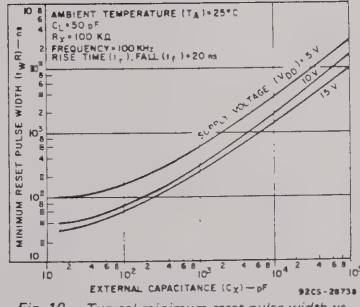


Fig. 10 – Typical minimum reset pulse width vs. external capacitance.

TEST CIRCUITS

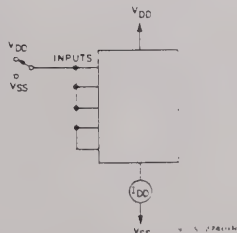


Fig. 12 – Quiescent device current test circuits.

DYNAMIC ELECTRICAL CHARACTERISTICS

At $T_A = 25^{\circ}\text{C}$; Input $t_r, t_f = 20\text{ ns}$, $C_L = 50\text{ pF}$, $R_L = 200\text{ k}\Omega$

CHARACTERISTIC	TEST CONDITIONS			LIMITS		UNITS
	$R_X\text{ (k}\Omega\text{)}$	$C_X\text{ (pF)}$	$V_{DD}\text{ (V)}$	Typ.	Max.	
Trigger Propagation Delay Time $+TR, -TR$ to Q, \bar{Q} t_{PHL}, t_{PLH}	5 to 10,000	≥ 15	5 10 15	250 125 100	500 250 200	ns
Minimum Trigger Pulse Width, t_{WH}, t_{WL}	5 to 10,000	≥ 15	5 10 15	70 30 20	140 60 40	ns
Transition Time, t_{TLH}	5 to 10,000	≥ 15	5 10 15	100 50 40	200 100 80	ns
t_{THL}	5 to 10,000	15 to 10,000	5 10 15	100 50 40	200 100 80	
	5 to 10,000	0.01 μF to 0.1 μF	5 10 15	150 75 65	300 150 130	
	5 to 10,000	0.1 μF to 1 μF	5 10 15	250 150 80	500 300 160	
Reset Propagation Delay Time, T_{PHL}, T_{PLH}	5 to 10,000	≥ 15	5 10 15	225 125 75	450 250 150	ns
Minimum Reset Pulse Width, t_{WR}	100	15	5 10 15	100 40 30	200 80 60	ns
			5 10 15	600 300 250	1200 600 500	
			5 10 15	25 15 10	50 30 20	μs
		0.1 μF	5 10 15	25 15 10	50 30 20	
Trigger Rise or Fall Time $t_r(\text{TR}), t_f(\text{TR})$	—	—	5 to 15	—	100	μs
Pulse Width Match Between Circuits in Same Package	10	10,000	5 10 15	5 7.5 7.5	10 15 15	%
Input Capacitance, C_{IN}	Any Input			5	7.5	pF

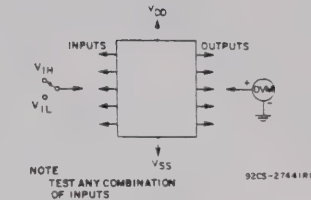


Fig. 13 - Input-voltage test circuit.

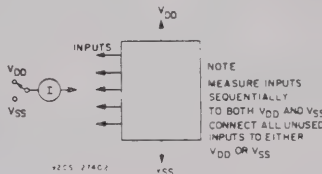


Fig. 14 - Input leakage current test circuit.

APPLICATIONS

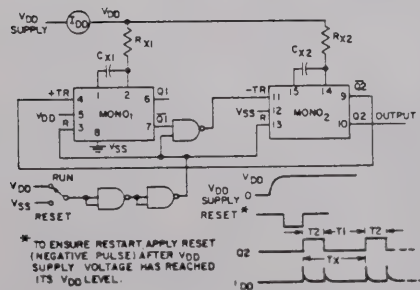


Fig. 15 - Astable multivibrator with restart after reset capability.

$I_{DD}, T_X \text{ vs. } R_X$			
R_X	$I_{DD}\text{ (Amp.)}$	$T_X\text{ (}\mu\text{s)}$ ($T_1 + T_2$)	V_{DD}
10 k Ω	1 mA	3.8 μs	5 V
	0.05 mA	0.5 μs	
	2.5 mA	3.2 μs	10 V
	0.5 mA	0.5 μs	
10 M Ω	5 mA	3 μs	15 V
	1 mA	0.5 μs	

Note:
All values are typical.
 C_X range: 0.0001 μF to 0.1 μF .
92CM-28740

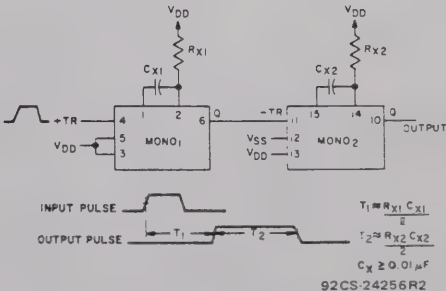


Fig. 16 - Pulse delay.

Preliminary Data

COS/MOS Presettable Divide-By-'N' Counter

High-Voltage Types (20-Volt Rating)

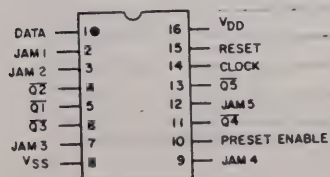
The RCA-CD4018B types consist of 5 Johnson-Counter stages, buffered \bar{Q} outputs from each stage, and counter preset control gating. CLOCK, RESET, DATA, PRESET ENABLE, and 5 individual JAM inputs are provided. Divide by 10, 8, 6, 4, or 2 counter configurations can be implemented by feeding the $\bar{Q}_5, \bar{Q}_4, \bar{Q}_3, \bar{Q}_2, \bar{Q}_1$ signals, respectively, back to the DATA input. Divide-by-9, 7, 5, or 3 counter configurations can be implemented by the use of a CD4011B gate package to properly gate the feedback connection to the DATA input. Divide-by functions greater than 10 can be achieved by use of multiple CD4018B units. The counter is advanced one count at the positive clock-signal transition. Schmitt Trigger action on the clock line permits unlimited clock rise and fall times. A high RESET signal clears the counter to an all-zero condition. A high PRESET-ENABLE signal allows information on the JAM inputs to preset the counter. Anti-lock gating is provided to assure the proper counting sequence.

The CD4018B-series types are supplied in 16-lead hermetic dual-in-line ceramic packages (D and F suffixes), 16-lead dual-in-line plastic packages (E suffix), 16-lead ceramic flat packages (K suffix), and in chip form (H suffix).

Applications:

- Fixed and programmable divide-by-10, 9, 8, 7, 6, 5, 4, 3, 2 counters
- Fixed and programmable counters greater than 10
- Programmable decade counters
- Divide-by-"N" counters/frequency synthesizers
- Frequency division
- Counter control/timers

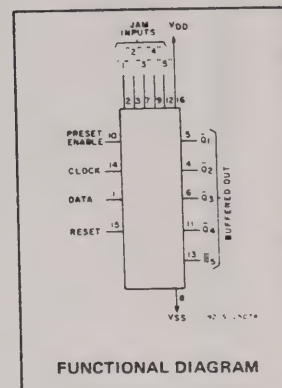
TERMINAL DIAGRAM
Top View



92C5-24460

Features:

- Medium speed operation 10 MHz (typ.) at $V_{DD} - V_{SS} = 10\text{ V}$
- Fully static operation
- 100% tested for quiescent current at 20 V
- Standardized, symmetrical output characteristics
- 5-V, 10-V, and 15-V parametric ratings
- Meets all requirements of JEDEC Tentative Standard No. 13A, "Standard Specifications for Description of 'B' Series CMOS Devices"



RECOMMENDED OPERATING CONDITIONS

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range (For T_A = Full Package Temperature Range)	3	18	V

STATIC ELECTRICAL CHARACTERISTICS

CHARACTER- ISTIC	CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C)							UNITS
				Values at -55, +25, +125 Apply to D,K,F,H Packages Values at -40, +25, +85 Apply to E Package							
	V _O (V)	V _{IN} (V)	V _{DD} (V)					+25			
-55				-40	+85	+125	Min.	Typ.	Max.		
Quiescent Device Current, I _{DD} Max.	—	0,5	5	5	5	150	150	—	0.04	5	μA
	—	0,10	10	10	10	300	300	—	0.04	10	
	—	0,15	15	20	20	600	600	—	0.04	20	
	—	0,20	20	100	100	3000	3000	—	0.08	100	
Output Low (Sink) Current I _{OL} Min.	0.4	0,5	5	0.64	0.61	0.42	0.36	0.51	1	—	mA
	0.5	0,10	10	1.6	1.5	1.1	0.9	1.3	2.6	—	
	1.5	0,15	15	4.2	4	2.8	2.4	3.4	6.8	—	
Output High (Source) Current, I _{OH} Min.	4.6	0,5	5	-0.64	-0.61	-0.42	-0.36	-0.51	-1	—	mA
	2.5	0,5	5	-2	-1.8	-1.3	-1.15	-1.6	-3.2	—	
	9.5	0,10	10	-1.6	-1.5	-1.1	-0.9	-1.3	-2.6	—	
	13.5	0,15	15	-4.2	-4	-2.8	-2.4	-3.4	-6.8	—	
Output Voltage: Low-Level, V _{OL} Max.	—	0,5	5	0.05				—	0	0.05	V
	—	0,10	10	0.05				—	0	0.05	
	—	0,15	15	0.05				—	0	0.05	
Output Voltage: High-Level, V _{OH} Min.	—	0,5	5	4.95				4.95	5	—	V
	—	0,10	10	9.95				9.95	10	—	
	—	0,15	15	14.95				14.95	15	—	
Input Low Voltage, V _{IL} Max.	0.5, 4.5	—	5	1.5				—	—	1.5	V
	1, 9	—	10	3				—	—	3	
	15, 13.5	—	15	4				—	—	4	
Input High Voltage, V _{IH} Min.	0.5, 4.5	—	5	3.5				3.5	—	—	V
	1, 9	—	10	7				7	—	—	
	1.5, 3.5	—	15	11				11	—	—	
Input Current I _{IN} Max.		0,18	18	±0.1	±0.1	±1	±1	—	±10 ⁻⁵	±0.1	μA



CD4018B Types

MAXIMUM RATINGS, Absolute-Maximum Values:

DC SUPPLY-VOLTAGE RANGE, (V_{DD}) (Voltages referenced to V_{SS} Terminal)	-0.5 to +20 V
INPUT VOLTAGE RANGE, ALL INPUTS	-0.5 to V_{DD} +0.5 V
DC INPUT CURRENT, ANY ONE INPUT	± 10 mA
POWER DISSIPATION PER PACKAGE (P_D):	
For $T_A = -40$ to $+60^\circ\text{C}$ (PACKAGE TYPE E)	500 mW
For $T_A = +60$ to $+85^\circ\text{C}$ (PACKAGE TYPE E)	Derate Linearly at 12 mW/ $^\circ\text{C}$ to 200 mW
For $T_A = -55$ to $+100^\circ\text{C}$ (PACKAGE TYPES D, F, K)	500 mW
For $T_A = +100$ to $+125^\circ\text{C}$ (PACKAGE TYPES D, F, K)	Derate Linearly at 12 mW/ $^\circ\text{C}$ to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR	
FOR $T_A =$ FULL PACKAGE-TEMPERATURE RANGE (All Package Types)	100 mW
OPERATING-TEMPERATURE RANGE (T_A):	
PACKAGE TYPES D, F, K, H	-55 to $+125^\circ\text{C}$
PACKAGE TYPE E	-40 to $+85^\circ\text{C}$
STORAGE TEMPERATURE RANGE (T_{stg})	-65 to $+150^\circ\text{C}$
LEAD TEMPERATURE (DURING SOLDERING):	
At distance 1/16 \pm 1/32 inch (1.59 \pm 0.79 mm) from case for 10 s max.	$+265^\circ\text{C}$

DYNAMIC ELECTRICAL CHARACTERISTICS at $T_A = 25^\circ\text{C}$, Input $t_r, t_f = 20$ ns,
 $C_L = 50$ pF, $R_L = 200$ k Ω

CHARACTERISTIC	TEST CONDITIONS		TYPICAL VALUES	UNITS
		V _{DD} (V)		
CLOCKED OPERATION				
Propagation Delay Time; t _{PLH} , t _{PHL}		5	180	ns
		10	90	
		15	60	
Transition Time; t _{THL} , t _{TLH}		5	100	ns
		10	50	
		15	40	
Maximum Clock Input Frequency, f _{CL}		5	5	MHz
		10	10	
		15	15	
Min. Clock Pulse Width, t _W		5	80	ns
		10	35	
		15	25	
Clock Rise & Fall Time; t _{rCL} , t _{fCL}		5	Unlimited	μs
		10		
		15		
Min. Data Input Set-Up Time, t _S		5	0	ns
		10	0	
		15	0	
Min. Data Input Hold Time, t _H		5	70	ns
		10	40	
		15	30	
Average Input Capacitance, C _I	Any Input		5	pF
PRESET* OR RESET OPERATION				
Propagation Delay Time; Reset or Reset to Q̄ t _{PLH} , t _{PHL}		5	280	ns
		10	120	
		15	80	
Min. Preset or Reset Pulse Width t _W		5	130	ns
		10	60	
		15	40	
Min. Preset or Reset Removal Time		5	70	ns
		10	30	
		15	20	

* At PRESET ENABLE OR JAM Inputs.

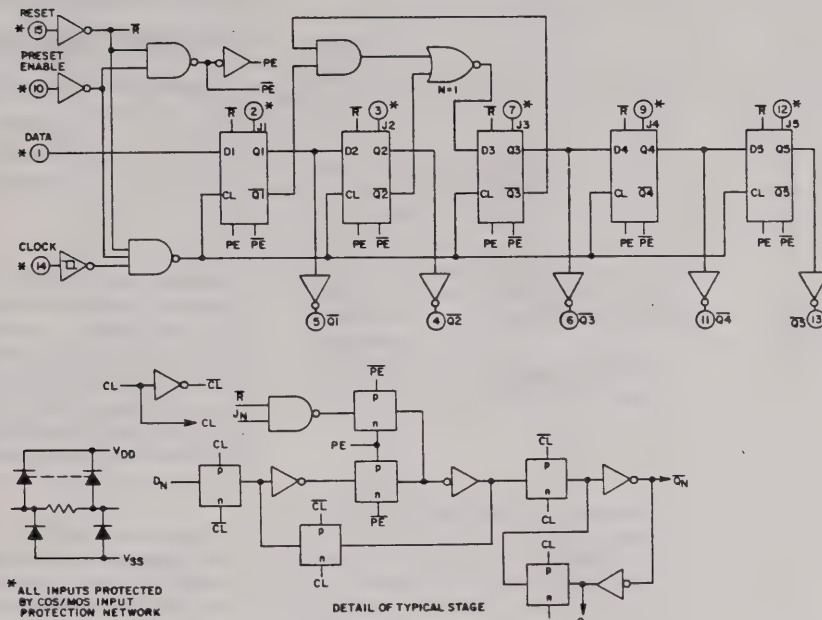


Fig. 1 - logic diagram.

("DATA" INPUT TIED TO \bar{Q}_5 FOR DECADE COUNTER CONFIGURATION)

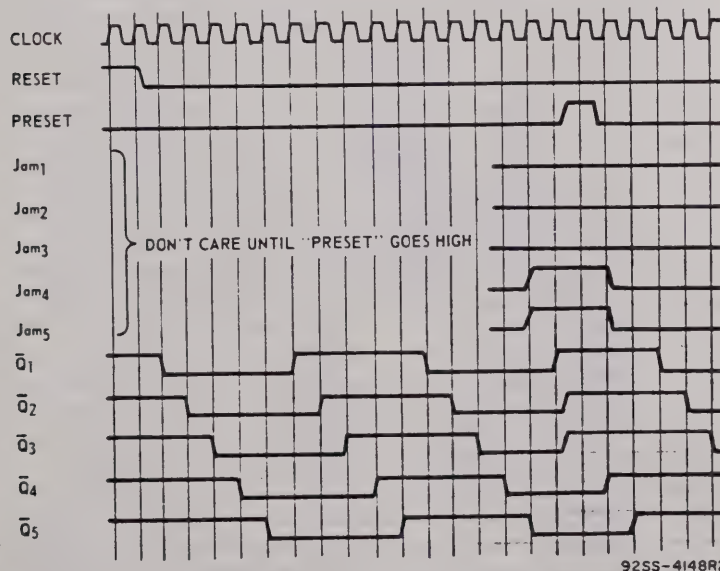


Fig. 2 - Timing diagram.

EXTERNAL CONNECTIONS FOR DIVIDE BY 10, 9, 8, 7, 6, 5, 4, 3 OPERATION

DIVIDE BY 10	\bar{Q}_5	CONNECTED BACK TO "DATA" } NO EXTERNAL COMPONENTS REQUIRED
DIVIDE BY 8	\bar{Q}_4	
DIVIDE BY 6	\bar{Q}_3	
DIVIDE BY 4	\bar{Q}_2	
DIVIDE BY 2	\bar{Q}_1	

DIVIDE BY 9



DIVIDE BY 7



DIVIDE BY 5



DIVIDE BY 3



92CS-17071R3

Fig. 3 - External connections for divide by 10, 9, 8, 7, 6, 5, 4, 3, 2 operation.

CD4020B, CD4024B, CD4040B Types

C^{MOS} Ripple-Carry Binary Counter/Dividers

Preliminary Data

High-Voltage Types (20-Volt Rating)

CD4020B — 14 Stage

CD4024B — 7 Stage

CD4040B — 12 Stage

RCA-CD4020B, CD4024B, and CD4040B are ripple-carry binary counters. All counter stages are master-slave flip-flops. The state of a counter advances one count on the negative transition of each input pulse; a high level on the RESET line resets the counter to its all zeros state. Schmitt trigger action on the input-pulse line permits unlimited clock rise and fall times. All inputs and outputs are buffered.

The CD4020B, CD4024B and CD4040B-series types are supplied in 16-lead ceramic dual-in-line packages (D and F suffixes), 16-lead dual-in-line plastic packages (K suffix), and in chip form (H suffix).

Features:

- Medium-speed operation
- Fully static operation
- Common reset
- Buffered inputs and outputs
- 100% tested for quiescent current at 20 V
- Standardized, symmetrical output characteristics
- 5-V, 10-V, and 15-V parametric ratings
- Meets all requirements of JEDEC Tentative Standard No. 13A, "Standard Specifications for Description of 'B' Series CMOS Devices"

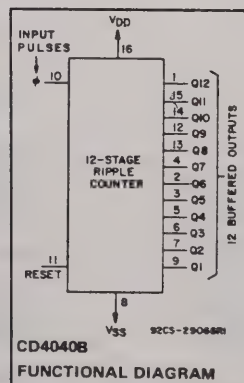
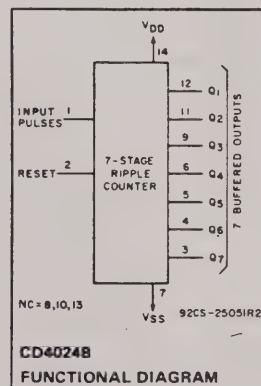
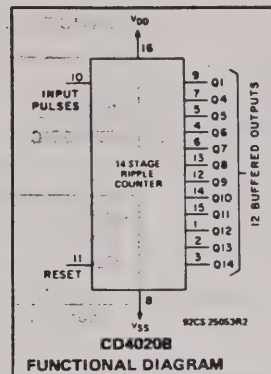
Applications:

- Control counters
- Frequency dividers
- Timers
- Time-delay circuits

The CD4024B-series types are supplied in 14-lead hermetic dual-in-line ceramic packages (D and F suffixes), 14-lead dual-in-line plastic packages (E suffix), 14-lead ceramic flat packages (K suffix), and in chip form (H suffix).

STATIC ELECTRICAL CHARACTERISTICS

CHARACTER- ISTIC	CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C)								UNITS
	V _O (V)	V _{IN} (V)	V _{DD} (V)	Values at -55, +25, +125 Apply to D,K,F,H Packages Values at -40, +25, +85 Apply to E Package								
				-55	-40	+85	+125	+25				
								Min.	Typ.	Max.		
Quiescent Device Current, I _{DD} Max.	—	0,5	5	5	5	150	150	—	0.04	5	μA	
	—	0,10	10	10	10	300	300	—	0.04	10		
	—	0,15	15	20	20	600	600	—	0.04	20		
	—	0,20	20	100	100	3000	3000	—	0.08	100		
Output Low (Sink) Current I _{OL} Min.	0.4	0,5	5	0.64	0.61	0.42	0.36	0.51	1	—	mA	
	0.5	0,10	10	1.6	1.5	1.1	0.9	1.3	2.6	—		
	1.5	0,15	15	4.2	4	2.8	2.4	3.4	6.8	—		
Output High (Source) Current, I _{OH} Min.	4.6	0,5	5	-0.64	-0.61	-0.42	-0.36	-0.51	-1	—	mA	
	2.5	0,5	5	-2	-1.8	-1.3	-1.15	-1.6	-3.2	—		
	9.5	0,10	10	-1.6	-1.5	-1.1	-0.9	-1.3	-2.6	—		
	13.5	0,15	15	-4.2	-4	-2.8	-2.4	-3.4	-6.8	—		
Output Voltage: Low-Level, V _{OL} Max.	—	0,5	5	0.05				—	0	0.05	V	
	—	0,10	10	0.05				—	0	0.05		
	—	0,15	15	0.05				—	0	0.05		
Output Voltage: High-Level, V _{OH} Min.	—	0,5	5	4.95				4.95	5	—	V	
	—	0,10	10	9.95				9.95	10	—		
	—	0,15	15	14.95				14.95	15	—		
Input Low Voltage, V _{IL} Max.	0.5, 4.5	—	5	1.5				—	—	1.5	V	
	1, 9	—	10	3				—	—	3		
	1.5, 13.5	—	15	4				—	—	4		
Input High Voltage, V _{IH} Min.	0.5, 4.5	—	5	3.5				3.5	—	—	V	
	1, 9	—	10	7				7	—	—		
	1.5, 13.5	—	15	11				11	—	—		
Input current I _{IN} Max.		0,18	18	±0.1	±0.1	±1	±1	—	±10 ⁻⁵	±0.1	μA	



CD4020B, CD4024B, CD4040B Types

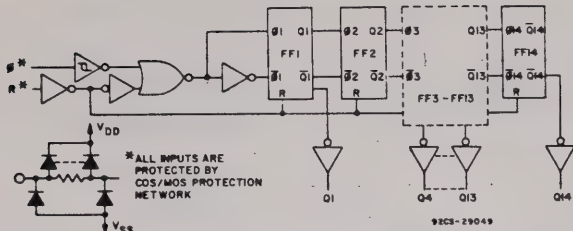


Fig. 1 — Logic diagram for CD4020B.

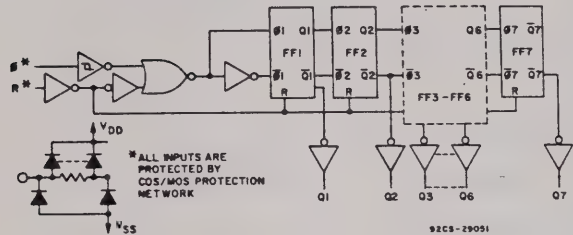


Fig. 2 — Logic diagram for CD4024B.

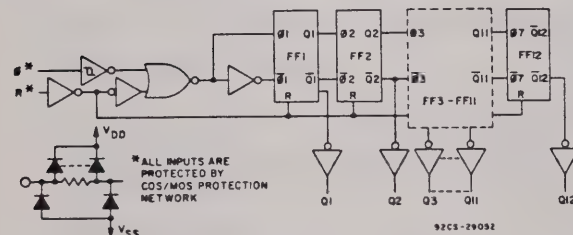


Fig. 3 — Logic diagram for CD4040B.

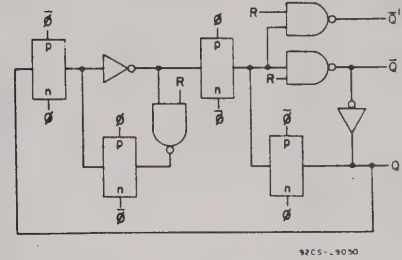
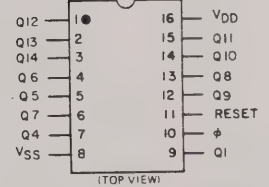


Fig. 4 — Detail of typical flip-flop stage.

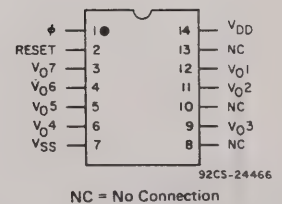
TERMINAL ASSIGNMENT

Top View

CD4020B



CD4024B



NC = No Connection

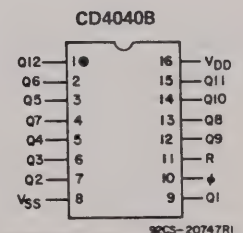
RECOMMENDED OPERATING CONDITIONS

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range (For $T_A =$ Full Package-Temperature Range)	3	18	V

MAXIMUM RATINGS, Absolute-Maximum Values:

DC SUPPLY-VOLTAGE RANGE, V_{DD} (Voltages referenced to V_{SS} terminal)	−0.5 to +20 V
INPUT VOLTAGE RANGE, ALL INPUTS	−0.5 to $V_{DD} + 0.5$ V
POWER DISSIPATION PER PACKAGE (P_D):	
For $T_A = -40$ to $+60^\circ\text{C}$ (Package Type E)	500 mW
For $T_A = +60$ to $+85^\circ\text{C}$ (Package Type E)	Derate Linearly to 200 mW
For $T_A = -55$ to $+100^\circ\text{C}$ (Package Types D,K,H)	500 mW
For $T_A = +100$ to $+125^\circ\text{C}$ (Package Types D,K,H)	Derate Linearly to 100 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR:	
For $T_A =$ Full package-temperature range (All package types)	100 mW
OPERATING-TEMPERATURE RANGE (T_A):	
Package Types D,K,H	−55 to $+125^\circ\text{C}$
Package Type E	−40 to $+85^\circ\text{C}$
STORAGE-TEMPERATURE RANGE (T_{STG})	−65 to $+150^\circ\text{C}$
LEAD TEMPERATURE (During Soldering):	
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max.	+265°C



CD4020B, CD4024B, CD4040B Types

DYNAMIC ELECTRICAL CHARACTERISTICS at $T_A = 25^\circ\text{C}$, Input $t_r, t_f = 20\text{ ns}$,
 $C_L = 50\text{ pF}$, $R_L = 200\text{ k}\Omega$

CHARACTERISTIC	TEST CONDITIONS	LIMITS		UNITS
		V _{DD} (V)	TYPICAL VALUES	
Input-Pulse Operation				
Propagation Delay Time, ϕ_1 to Q_1 Out; t_{PHL}, t_{PLH}		5	400	ns
		10	170	
		15	120	
Propagation Delay Time, Q_n to $Q_n + 1$; t_{PHL}, t_{PLH}		5	200	ns
		10	85	
		15	60	
Transition Time, t_{THL}, t_{TLH}		5	100	ns
		10	50	
		15	40	
Minimum Input-Pulse Width, t_W	$f = 100 \text{ kHz}$	5	70	ns
		10	30	
		15	20	
Input-Pulse Rise or Fall Time, $t_{r\phi}, t_{f\phi}$		5	Unlimited	μs
		10		
		15		
Maximum Input-Pulse Frequency, f_ϕ		5	7	MHz
		10	16	
		15	24	
Input Capacitance, C_i	Any Input		5	pF
Reset Operation				
Propagation Delay Time, t_{PHL}		5	300	ns
		10	140	
		15	100	
Minimum Reset Pulse Width, t_W		5	375	ns
		10	200	
		15	150	

CD4051B, CD4052B, CD4053B Types

COS/MOS Analog Multiplexers/Demultiplexers*

With Logic-Level Conversion

High-Voltages Types (20-Volt Rating)

CD4051B — Single 8-Channel

CD4052B — Differential 4-Channel

CD4053B — Triple 2-Channel

RCA-CD4051B, CD4052B, and CD4053B analog multiplexers/demultiplexers are digitally controlled analog switches having low ON impedance and very low OFF leakage current. Control of analog signals up to 20 V peak-to-peak can be achieved by digital signal amplitudes of 4.5 to 20 V (if $V_{DD}-V_{SS} = 3$ V, a $V_{DD}-V_{EE}$ of up to 13 V can be controlled; for $V_{DD}-V_{EE}$ level differences above 13 V, a $V_{DD}-V_{SS}$ of at least 4.5 V is required). For example, if $V_{DD} = +5$ V, $V_{SS} = 0$, and $V_{EE} = -13.5$ V, analog signals from -13.5 V to $+4.5$ V can be controlled by digital inputs of 0 to 5 V. These multiplexer circuits dissipate extremely low quiescent power over the full $V_{DD}-V_{SS}$ and $V_{DD}-V_{EE}$ supply-voltage ranges, independent of the logic state of the control signals. When a logic "1" is present at the inhibit input terminal all channels are off.

The CD4051B is a single 8-channel multiplexer having three binary control inputs, A, B, and C, and an inhibit input. The three binary signals select 1 of 8 channels to be turned on, and connect one of the 8 inputs to the output.

The CD4052B is a differential 4-channel multiplexer having two binary control inputs, A and B, and an inhibit input. The two binary input signals select 1 of 4 pairs of channels to be turned on and connect the analog inputs to the outputs.

The CD4053B is a triple 2-channel multiplexer having three separate digital control inputs, A, B, and C, and an inhibit input. Each control input selects one of a pair of channels which are connected in a single-pole double-throw configuration.

The CD4051B, CD4052B, and CD4053B are supplied in 16-lead ceramic dual-in-line packages (D and F suffixes), 16-lead plastic dual-in-line packages (E suffix), 16-lead ceramic flat packages (K suffix), and in chip form (H suffix).

Applications:

- Analog and digital multiplexing and demultiplexing
- A/D and D/A conversion
- Signal gating

Features:

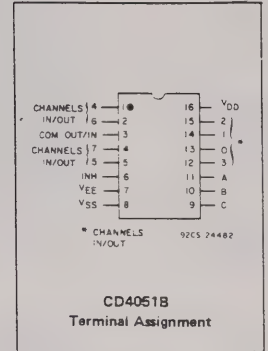
- Wide range of digital and analog signal levels: digital 3 to 20 V, analog to 20 V_{p-p}
- Low ON resistance: 125 Ω (typ.) over 15 V_{p-p} signal-input range for $V_{DD}-V_{EE} = 15$ V
- High OFF resistance: channel leakage of ± 100 pA (typ.) @ $V_{DD}-V_{EE} = 18$ V
- Logic-level conversion for digital addressing signals of 3 to 20 V ($V_{DD}-V_{SS} = 3$ to 20 V) to switch analog signals to 20 V p-p ($V_{DD}-V_{EE} = 20$ V); see introductory text
- Matched switch characteristics: $R_{ON} = 5$ Ω (typ.) for $V_{DD}-V_{EE} = 15$ V
- Very low quiescent power dissipation under all digital-control input and supply conditions: 0.2 μ W (typ.) @ $V_{DD}-V_{SS} = V_{DD}-V_{EE} = 10$ V
- Binary address decoding on chip
- 5-, 10-, and 15-V parametric ratings
- 100% tested for quiescent current at 20 V
- Maximum input current of 1 μ A at 18 V over full package temperature range; 100 nA at 18 V and 25°C
- Meets all requirements of JEDEC Tentative Standard No. 13A, "Standard Specifications for Description of 'B' Series CMOS Devices"

RECOMMENDED OPERATING CONDITIONS AT $T_A = 25^\circ\text{C}$ (Unless Otherwise Specified)

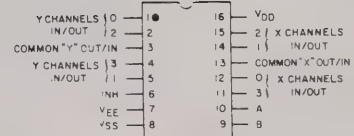
For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges. Values shown apply to all types except as noted.

CHARACTERISTIC	V_{DD}	Min.	Max.	Units
Supply-Voltage Range (T_A = Full Package-Temp. Range)	—	3	18	V
Multiplexer Switch Input Current Capability*	—	—	25	mA
Output Load Resistance	—	100	—	Ω

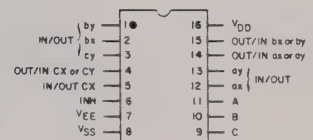
* In certain applications, the external load-resistor current may include both V_{DD} and signal-line components. To avoid drawing V_{DD} current when switch current flows into the transmission gate inputs, the voltage drop across the bidirectional switch must not exceed 0.8 volt (calculated from R_{ON} values shown in ELECTRICAL CHARACTERISTICS CHART). No V_{DD} current will flow through R_L if the switch current flows into terminal 3 on the CD4051; terminals 3 and 13 on the CD4052; terminals 4, 14, and 15 on the CD4053.



CD4051B
Terminal Assignment



CD4052B
Terminal Assignment



CD4053B
Terminal Assignment

* When these devices are used as demultiplexers, the "CHANNEL IN/OUT" terminals are the outputs and the "COMMON OUT/IN" terminals are the inputs.

CD4051B, CD4052B, CD4053B Types

MAXIMUM RATINGS, Absolute-Maximum Values:

DC SUPPLY-VOLTAGE RANGE, (V _{DD})	-0.5 to +20 V
(Voltages referenced to V _{SS} or V _{EE} , whichever is more negative)	
INPUT VOLTAGE RANGE, ALL INPUTS	-0.5 to V _{DD} +0.5 V
DC INPUT CURRENT, ANY ONE INPUT	±10 mA
POWER DISSIPATION PER PACKAGE (P _D):	
For T _A = -40 to +60°C (PACKAGE TYPE E)	500 mW
For T _A = +60 to +85°C (PACKAGE TYPE E)	Derate Linearly at 12 mW/°C to 200 mW
For T _A = -55 to +100°C (PACKAGE TYPES D, F, K)	500 mW
For T _A = +100 to +125°C (PACKAGE TYPES D, F, K)	Derate Linearly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR	
For T _A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types)	100 mW
OPERATING-TEMPERATURE RANGE (T _A):	
PACKAGE TYPES D, F, K, H	-55 to +125°C
PACKAGE TYPE E	-40 to +85°C
STORAGE TEMPERATURE RANGE (T _{stg})	-65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):	
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max.	+265°C

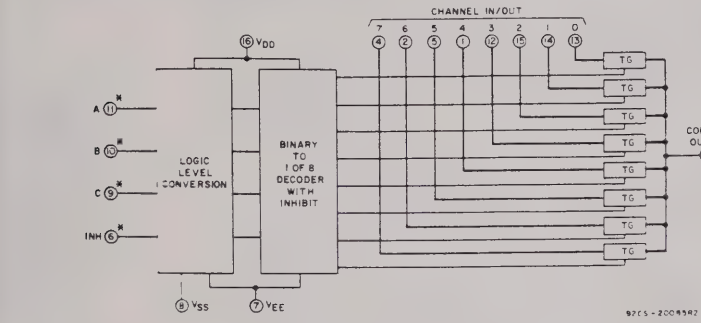


Fig. 1 - Functional diagram of CD4051B.

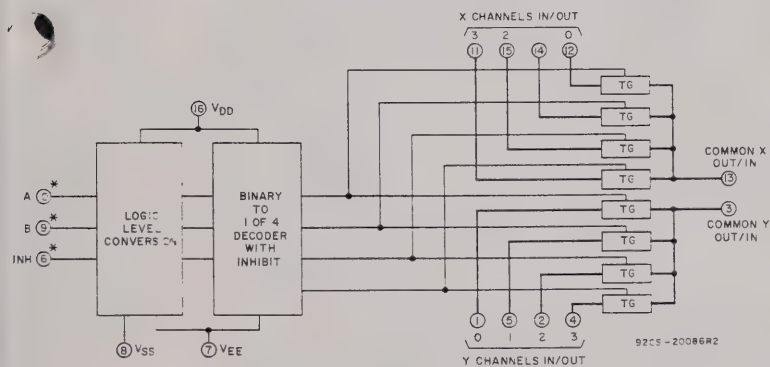


Fig. 2 - Functional diagram of CD4052B.

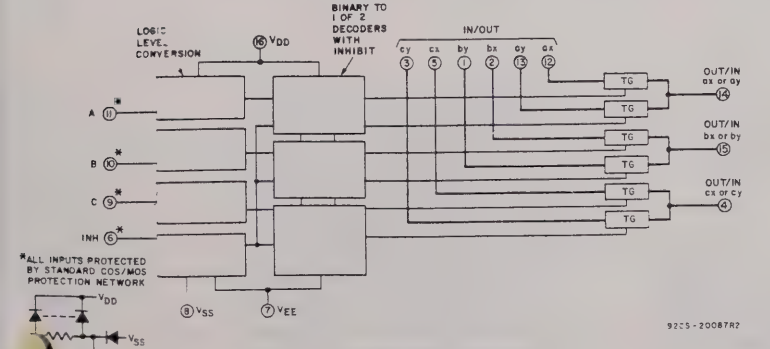


Fig. 3 - Functional diagram of CD4053B.

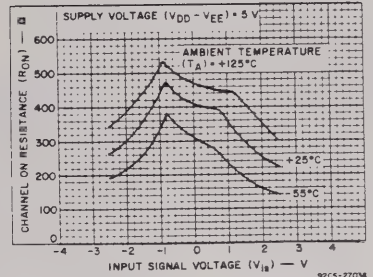


Fig. 4 - Typical channel ON resistance vs input signal voltage (all types).

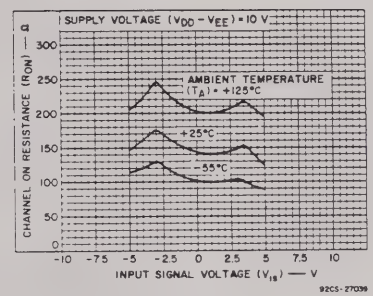


Fig. 5 - Typical channel ON resistance vs. input signal voltage (all types).

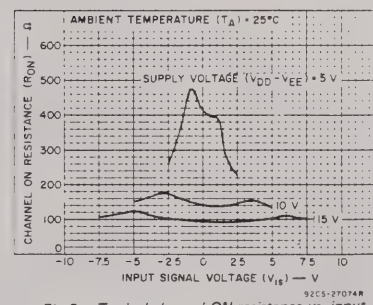


Fig. 6 - Typical channel ON resistance vs. input signal voltage (all types).

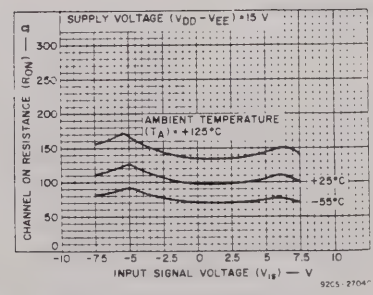
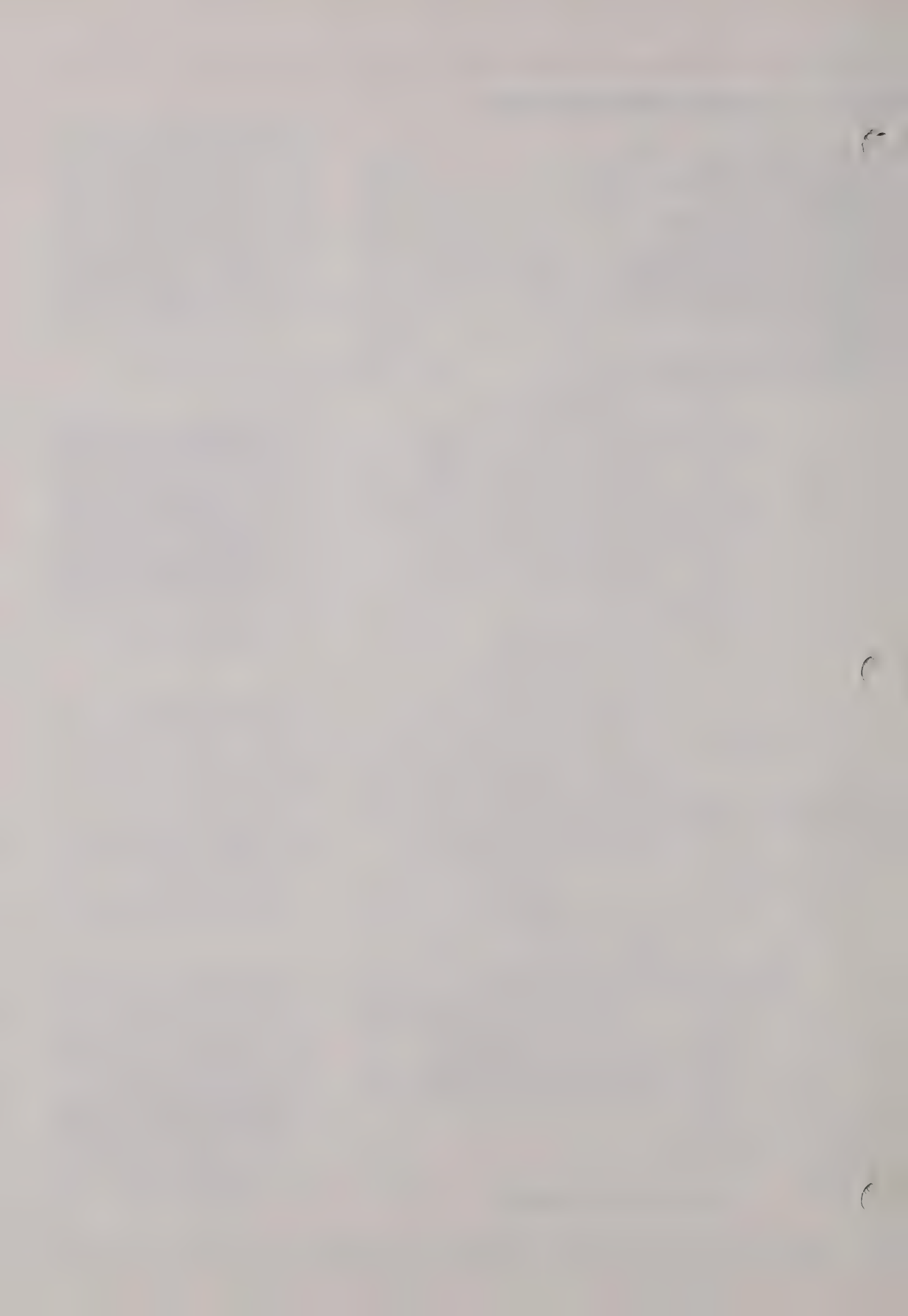


Fig. 7 - Typical channel ON resistance vs. input signal voltage (all types).



CD4051B, CD4052B, CD4053B Types

ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CONDITIONS				LIMITS at Indicated Temperature (°C)								Units
	V _{IS} (V)	V _{EE} (V)	V _{SS} (V)	V _{DD} (V)	Values at -55,+25,+125, apply to D,F,K,H pkg								
					Values at -40,+25,+85, apply to E pks								
					-55	-40	+85	+125	+25				
									Min.	Typ.	Max.		
SIGNAL INPUTS (V _{IS}) AND OUTPUTS (V _{OS})													
Quiescent Device Current, I _{DD} Max.				5	5	5	150	150	—	0.04	5	μA	
				10	10	10	300	300	—	0.04	10		
				15	20	20	600	600	—	0.04	20		
				20	100	100	3000	3000	—	0.08	100		
ON Resistance 0 ≤ V _{IS} ≤ V _{DD} R _{ON} Max.												Ω	
		0	0	5	2000	2100	3200	3500	—	470	2500		
		0	0	10	310	330	520	580	—	180	400		
		0	0	15	220	230	360	400	—	125	280		
Δ ON Resistance (Between Any Two Channels) Δ R _{ON}												Ω	
		0	0	5	—	—	—	—	—	10	—		
		0	0	10	—	—	—	—	—	10	—		
		0	0	15	—	—	—	—	—	5	—		
OFF Channel Leakage Current: Any Channel OFF Max. All Channels OFF (Common OUT/IN) Max.												nA	
		0	0	10	±200*			—	±0.01	±200*			
		0	0	15	±500*			—	±0.01	±200*			
		0	0	20	±1000*			—	±0.01	±200*			
		0	0	10	±200*			—	±0.01	±200*			
Capacitance: Input, C _{IS} Output, C _{OS} CD4051 CD4052 CD4053 Feedthrough, C _{IOS}												pF	
					—	—	—	—	—	5	—		
					—	—	—	—	—	30	—		
					—	—	—	—	—	18	—		
					—	—	—	—	—	9	—		
Propagation Delay Time (Signal Input to Output)												ns	
					—	—	—	—	—	0.2	—		
					—	—	—	—	—	—	—		
					—	—	—	—	—	—	—		
10V												ns	
					—	—	—	—	—	30	—		
					10	—	—	—	—	15	—		
					15	—	—	—	—	11	—		
R _L = 10 kΩ C _L = 50 pF tr,tf = 20 ns												ns	
					—	—	—	—	—	—	—		
					—	—	—	—	—	—	—		
					—	—	—	—	—	—	—		

* Determined by minimum feasible leakage measurement for automatic testing.

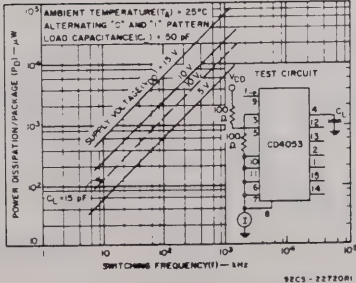
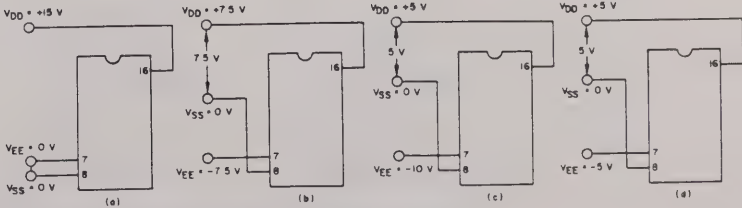


Fig.11 — Typical dynamic power dissipation vs. switching frequency (CD4053B).



The ADDRESS (digital-control inputs) and INHIBIT logic levels are: "0" = V_{SS} and "1" = V_{DD}. The analog signal (through the TG) may swing from V_{EE} to V_{DD}.

Fig.12 — Typical bias voltages.

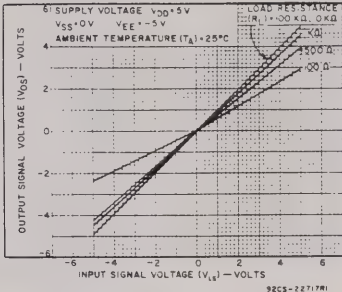


Fig.8 — Typical ON characteristics for 1 of 8 channels (CD4051B).

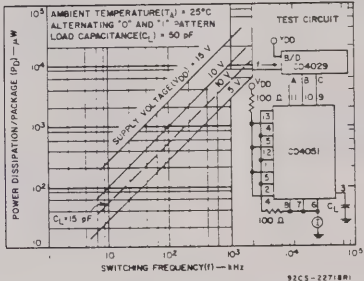


Fig.9 — Typical dynamic power dissipation vs. switching frequency (CD4051B).

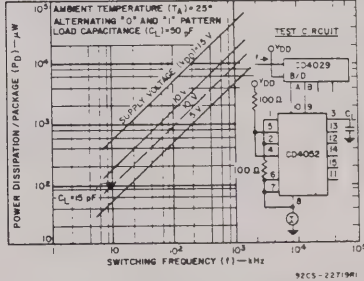
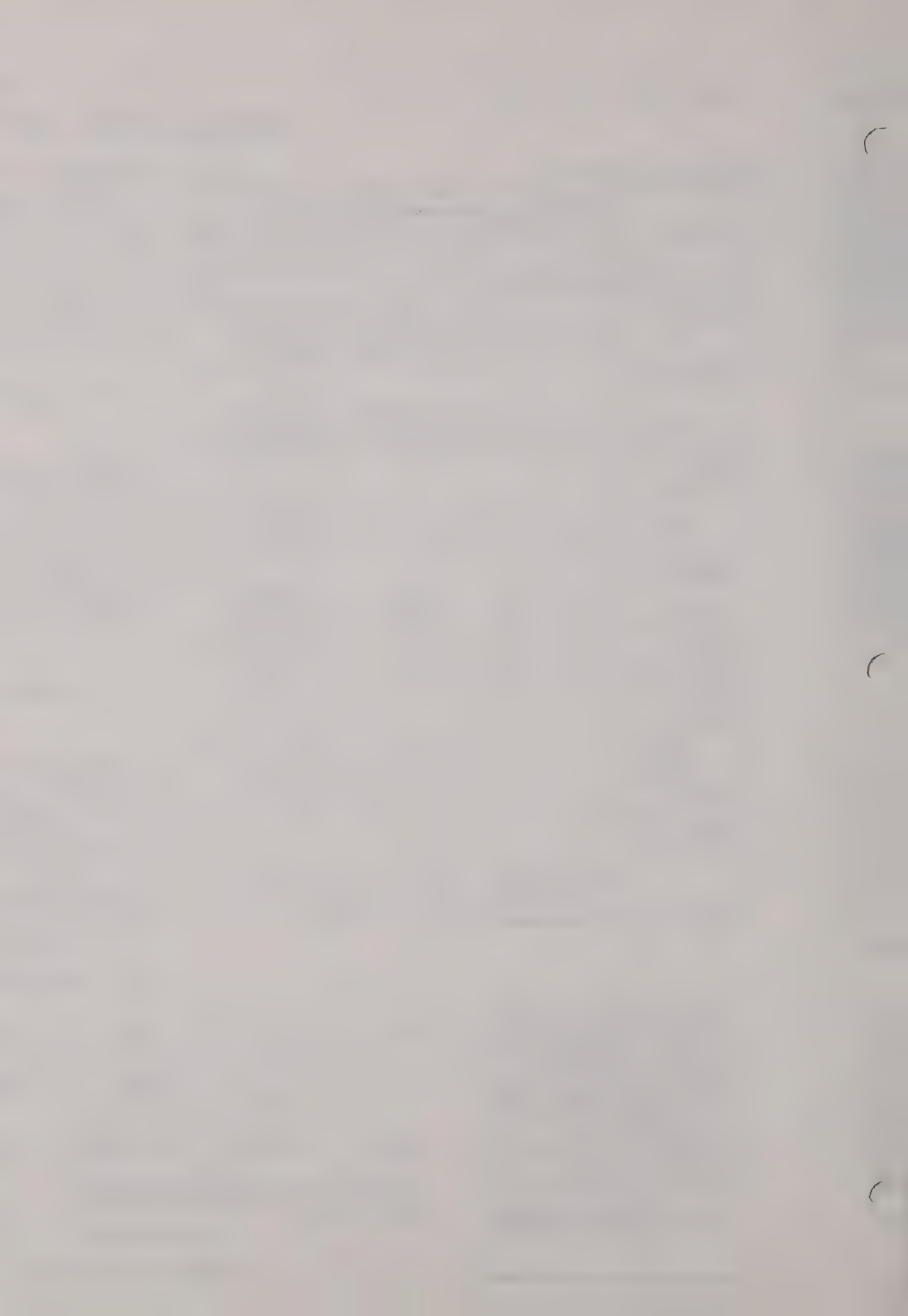


Fig.10 — Typical dynamic power dissipation vs. switching frequency (CD4052B).



CD4051B, CD4052B, CD4053B Types

ELECTRICAL CHARACTERISTICS (Cont'd)

CHARACTERISTIC	CONDITIONS				LIMITS at Indicated Temperature (°C)								Units
	V _{IS} (V)	V _{EE} (V)	V _{SS} (V)	V _{DD} (V)	Values at -55,+25,+125, apply to D,F,K,H pkg Values at -40,+25,+85, apply to E pkg								
					-55	-40	+85	+125	+25				
									Min.	Typ.	Max.		
CONTROL (ADDRESS or INHIBIT) V _C													
Input Low Voltage, V _{IL} Max.	=V _{DD} thru 1 kΩ	V _{EE} =V _{SS} R _L =1 kΩ to V _{SS} I _{IS} < 2 μA on all OFF Channels	5	1.5				—	—	1.5		V	
Input High Voltage, V _{IH} Min.			10	3				—	—	3			
			15	4				—	—	4			
			5	3.5				3.5		—			
			10	7				7		—			
			15	11				11		—			
Input Current, I _{IN} Max.		V _{IN} = 0.18	18	±0.1	±0.1	±1	±1	—	±10 ⁻⁵		±0.1	μA	
Propagation Delay Time:	t _r , t _f = 20 ns, C _L = 50 pF												
Address-to-Signal OUT (Channels ON or OFF) See Figs.14,15,18	0	0	5	—	—	—	—	—	360	720		ns	
	0	0	10	—	—	—	—	—	160	320			
	0	0	15	—	—	—	—	—	120	240			
	-5	0	5	—	—	—	—	—	225	450			
Inhibit-to-Signal OUT (Channel turning ON)	R _L =10 kΩ, C _L =50 pF t _r , t _f = 20 ns												
	0	0	5	—	—	—	—	—	360	720		ns	
	0	0	10	—	—	—	—	—	160	320			
	0	0	15	—	—	—	—	—	120	240			
	-10	0	5	—	—	—	—	—	200	400			
Inhibit-to-Signal OUT (Channel turning OFF)	R _L =300Ω, C _L =50 pF t _r , t _f = 20 ns												
	0	0	5	—	—	—	—	—	200	450		ns	
	0	0	10	—	—	—	—	—	90	210			
	0	0	15	—	—	—	—	—	70	160			
	-10	0	5	—	—	—	—	—	130	300			
Input Capacitance, C _{IN} (Any Address or Inhibit Input)				—	—	—	—	—	5	7.5		pF	

INPUT STATES				"ON" CHANNEL(S)
INHIBIT	C	B	A	
CD4051B				
0	0	0	0	0
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6
0	1	1	1	7
1	X	X	X	NONE
CD4052B				
INHIBIT	B	A		
0	0	0	0x, 0y	
0	0	1	1x, 1y	
0	1	0	2x, 2y	
0	1	1	3x, 3y	
1	X	X	NONE	
CD4053B				
INHIBIT	A or B or C			
0	0		ax or bx or cx	
0	1		ay or by or cy	
1	X		NONE	

X = Don't care
Fig. 13 — Truth tables.

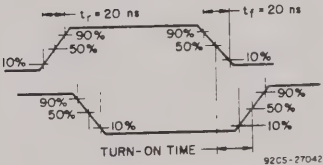


Fig. 14 — Waveforms, channel being turned ON (R_L = 10 kΩ).

TEST CIRCUITS

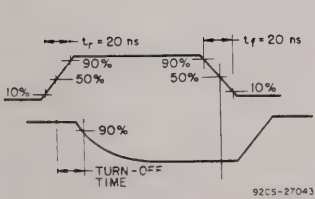


Fig. 15 — Waveforms, channel being turned OFF (R_L = 300 Ω).

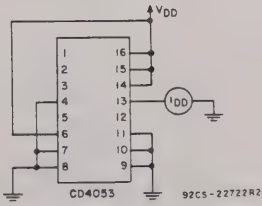
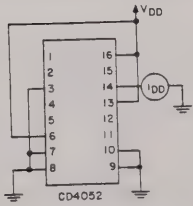
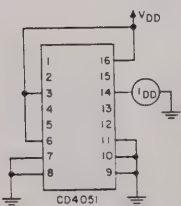
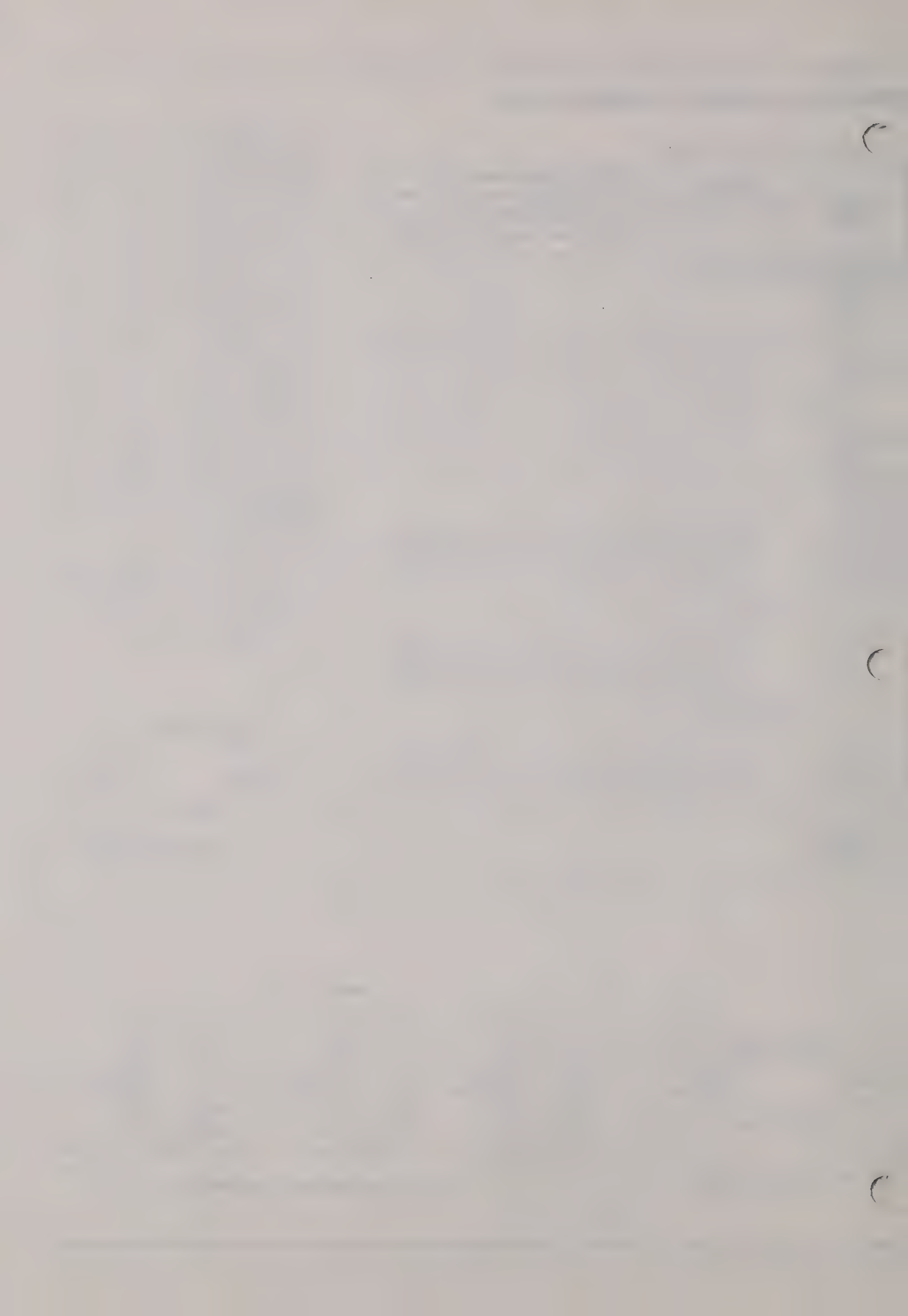


Fig. 16 — OFF channel leakage current — any channel OFF.



CD4051B, CD4052B, CD4053B Types

ELECTRICAL CHARACTERISTICS (Cont'd)

TEST CIRCUITS (Cont'd)

CHARACTERISTIC	TEST CONDITIONS					LIMITS	UNITS	
	V _{is} (V)	V _{DD} (V)	R _L (kΩ)			TYPICAL VALUE		
Frequency Response Channel ON (Sine Wave Input)	5 [●]	10	1			CD4053	30	MHz
	V _{EE} = V _{SS} .			V _{OS} at Common OUT/IN	CD4052	25		
	20 log $\frac{V_{OS}}{V_{is}}$ = -3 dB				CD4051	20		
				V _{OS} at Any Channel		60		
Sine Wave Response (Distortion)	2 [●]	5	10				0.3	%
	3 [●]	10			0.2			
	5 [●]	15			0.12			
	V _{EE} = V _{SS} , f _{is} = 1 kHz							
	Feedthrough (All Channels OFF)	5 [●]	10	1			CD4053	8
V _{EE} = V _{SS} .			V _{OS} at Common OUT/IN	CD4052	10			
20 log $\frac{V_{OS}}{V_{is}}$ = -40 dB				CD4051	12			
			V _{OS} at Any Channel		8			
Signal Crosstalk (Frequency at -40 dB)	5 [●]	10	1	Between Any 2 Channels			3	MHz
				Between Sections	Measured on Common		6	
					Measured on Any Channel		10	
	V _{EE} = V _{SS} .			CD4052 Only				
	20 log $\frac{V_{OS}}{V_{is}}$ = -40 dB			Between Any 2 Sections	In Pin 2, Out Pin 14		2.5	
				CD4053 Only	In Pin 15, Out Pin 14		6	
Address-or-Inhibit- to Signal Crosstalk	—	10	10 [#]				65	mV (Peak)
	V _{EE} =0, V _{SS} =0, t _r , t _f = 20 ns, V _C = V _{DD} -V _{SS} (Square Wave)							

● Peak-to-peak voltage symmetrical about $\frac{V_{DD} - V_{EE}}{2}$

Both ends of channel

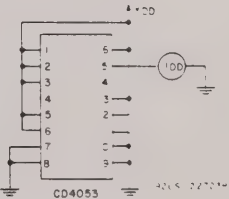
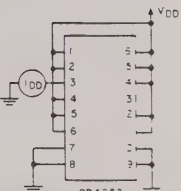
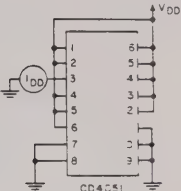


Fig.17 – OFF channel leakage current – all channels OFF.

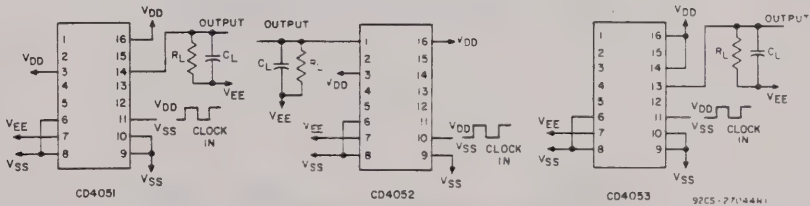


Fig.18 – Propagation delay – address input to signal output.

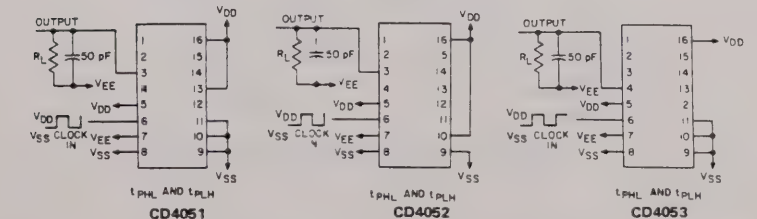


Fig.19 – Propagation delay – inhibit input to signal output.

CD4051B, CD4052B, CD4053B Types

TEST CIRCUITS (Cont'd)

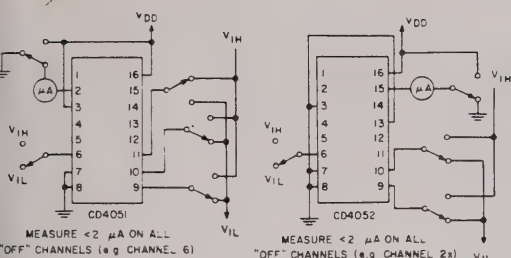


Fig. 20 - Input voltage.

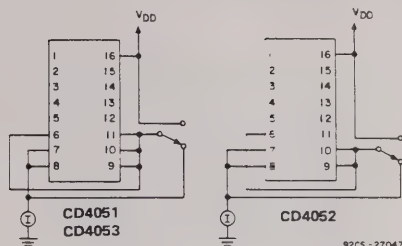


Fig. 21 - Quiescent device current.

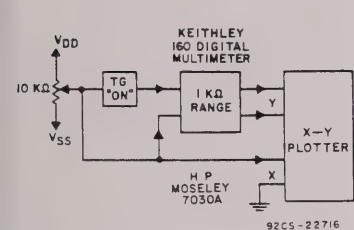


Fig. 22 - Channel ON resistance measurement circuit.

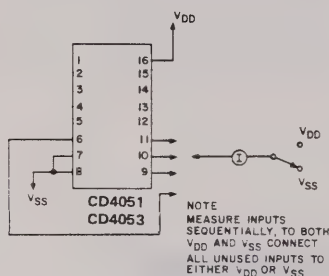
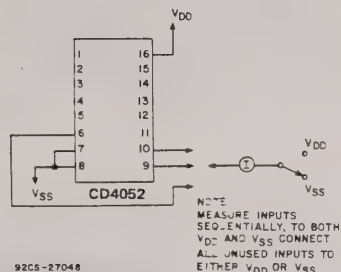
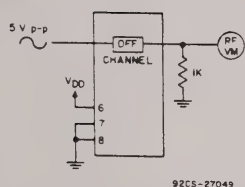


Fig. 23 - Input current.

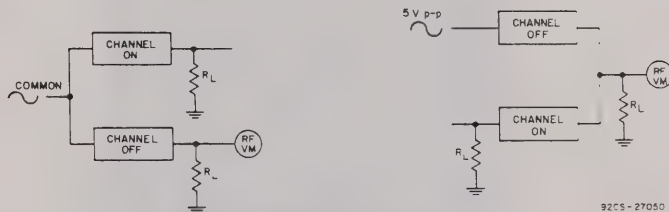


92CS-27048



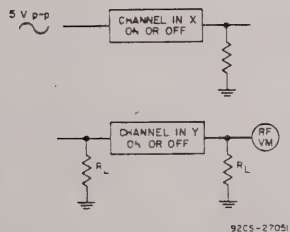
92CS-27049

Fig. 24 - Feedthrough (all types).



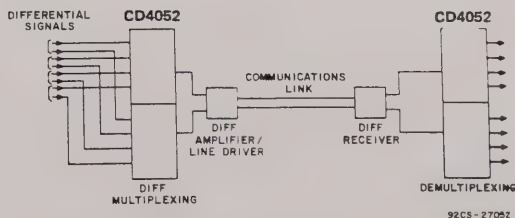
92CS-27050

Fig. 25 - Crosstalk between any two channels (all types).



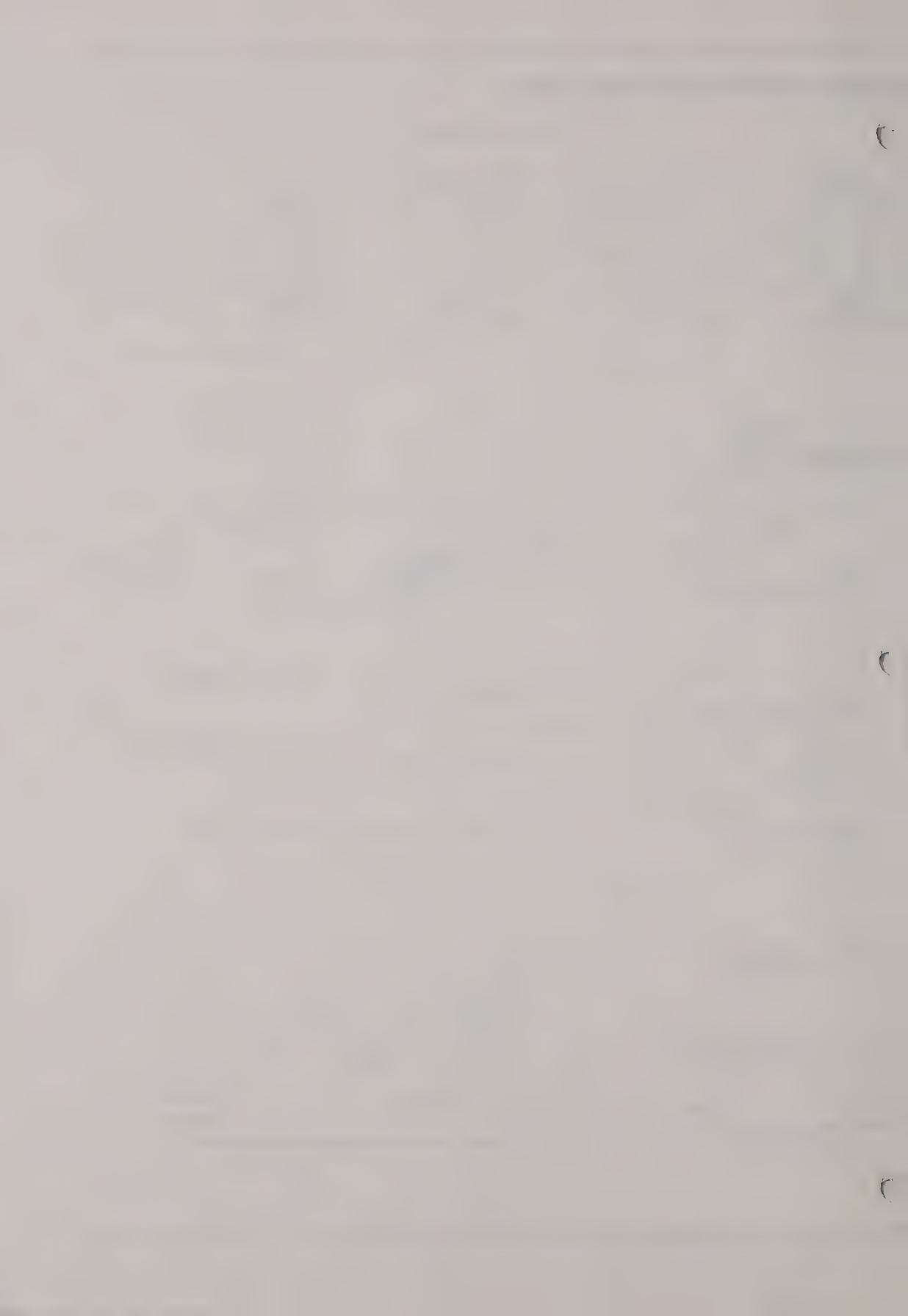
92CS-27051

Fig. 26 - Crosstalk between duals or triplets (CD4052B, CD4053B).



92CS-27052

Fig. 27 - Typical time-division application of the CD4052B.



CD4051B, CD4052B, CD4053B Types

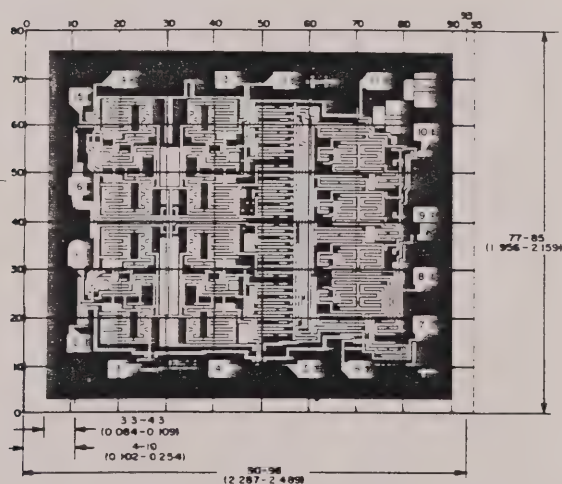
SPECIAL CONSIDERATIONS

In applications where separate power sources are used to drive V_{DD} and the signal inputs, the V_{DD} current capability should exceed V_{DD}/R_L (R_L = effective external load). This provision avoids permanent current flow or clamping action on the V_{DD} supply when power is applied or removed from the CD4051B, CD4052B, or CD4053B.

When switching from one address to another, some of the ON periods of the channels of the multiplexers will overlap momentarily, which may be objectionable in certain applications. Also when a channel is turned ON or OFF by an address input, there is a momentary conductive path from the channel to V_{EE} , which will dump some charge from any capacitor connected to the input or output of the channel. The inhibit input

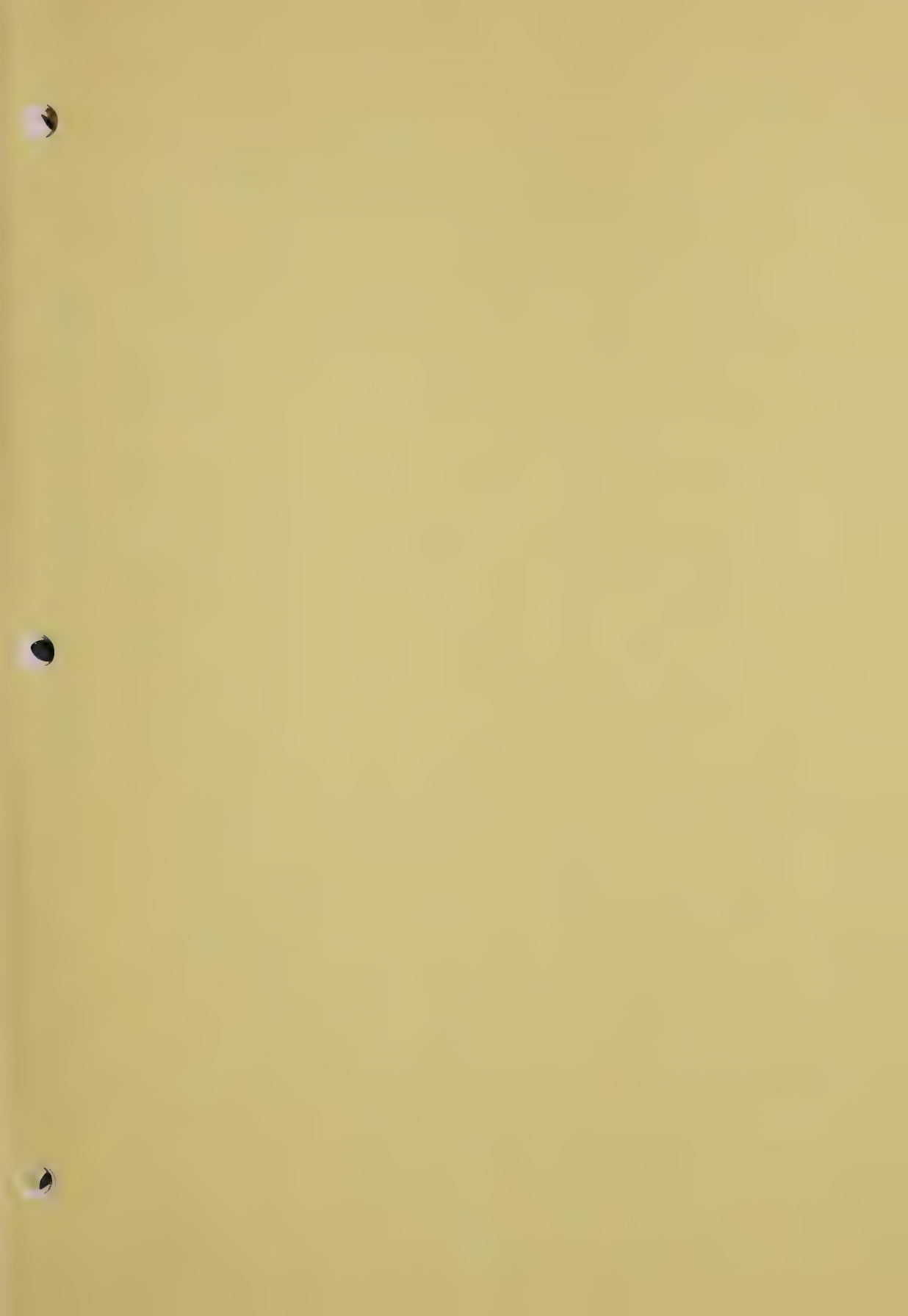
turning ON a channel will similarly dump some charge to V_{EE} .

The amount of charge dumped is mostly a function of the signal level above V_{EE} . Typically, at $V_{DD}-V_{EE} = 10$ V, a 100 pF capacitor connected to the input or output of the channel will lose 3-4 % of its voltage at the moment the channel turns ON or OFF. This loss of voltage is essentially independent of the address or inhibit signal transition time, if the transition time is less than 1-2 μ s. When the inhibit signal turns a channel OFF, there is no charge dumping to V_{EE} . Rather, there is a slight rise in the channel voltage level (65 mV typ.) due to capacitive coupling from inhibit input to channel input or output. Address inputs also couple some voltage steps onto the channel signal levels.

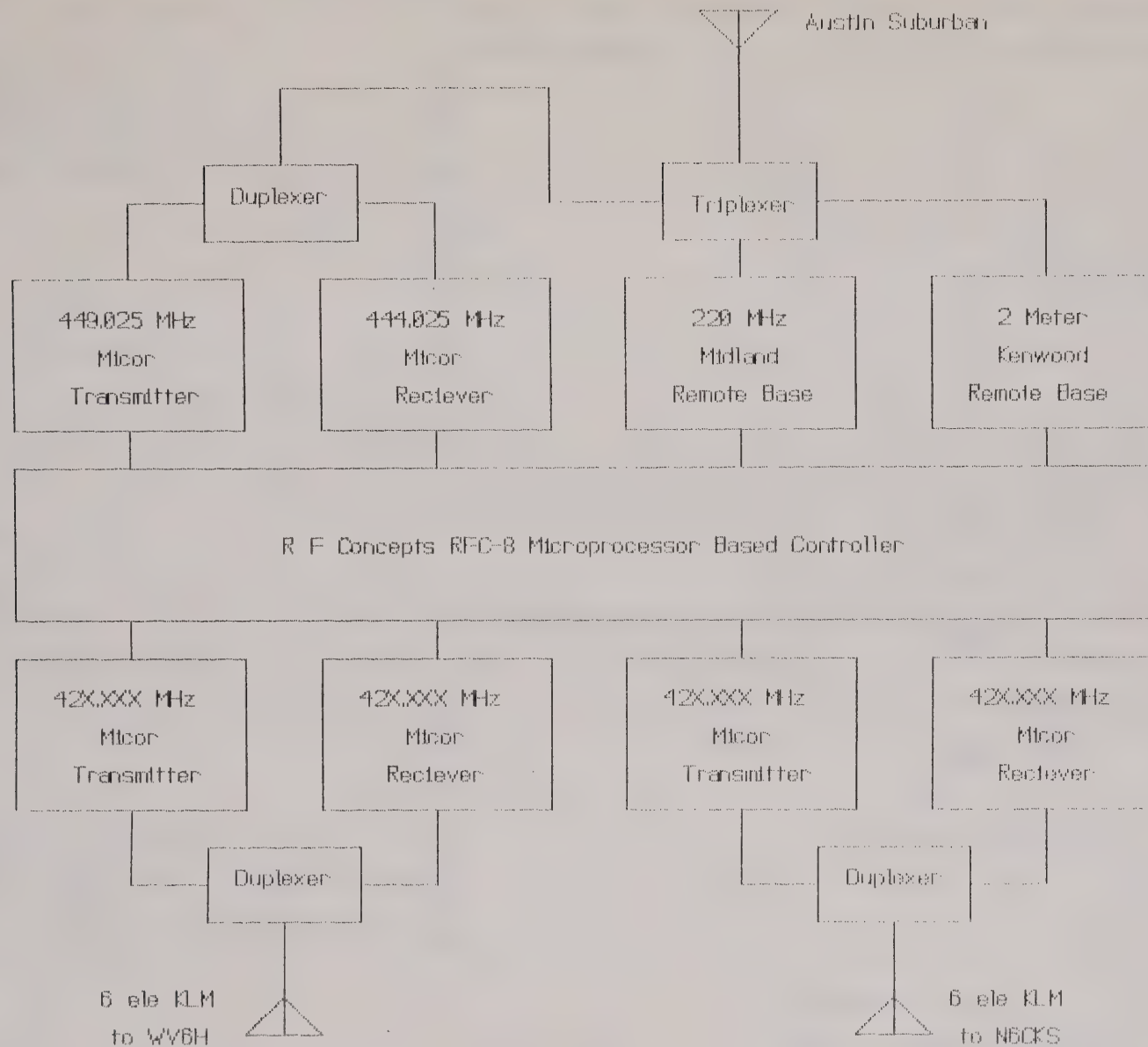


Dimensions and pad layout for CD4051B.

92C8-27093



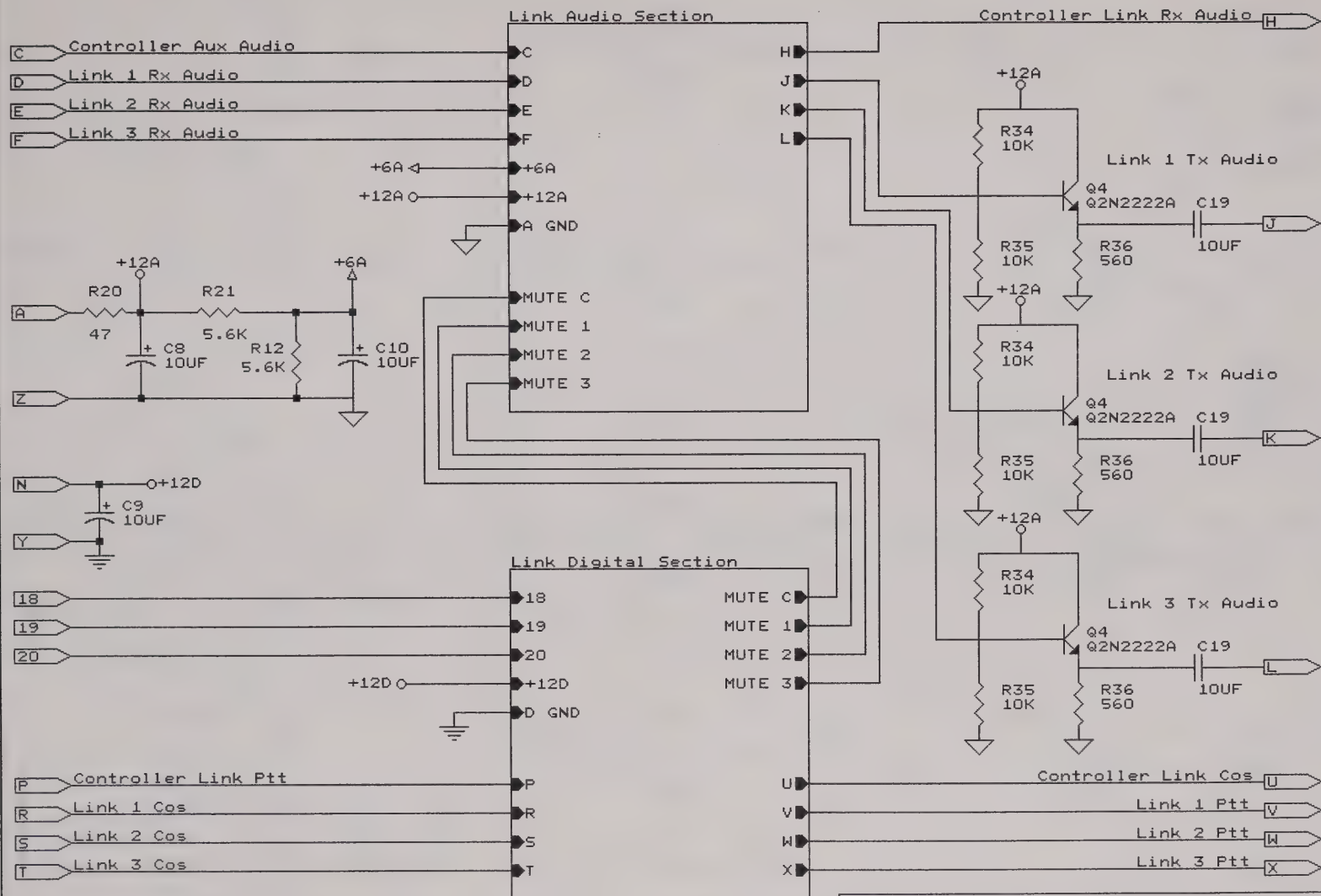
Hendrix Peak System Block Diagram

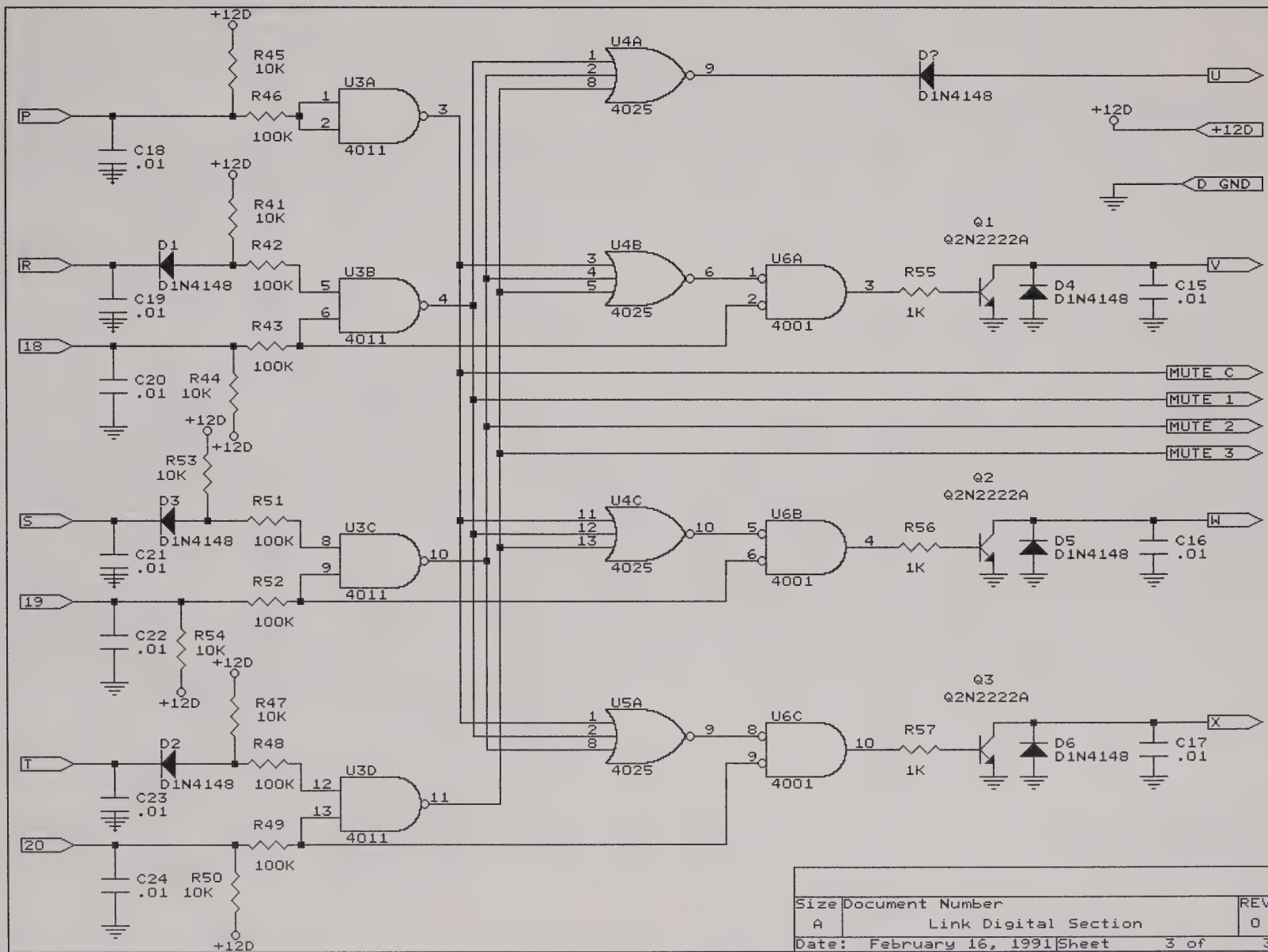


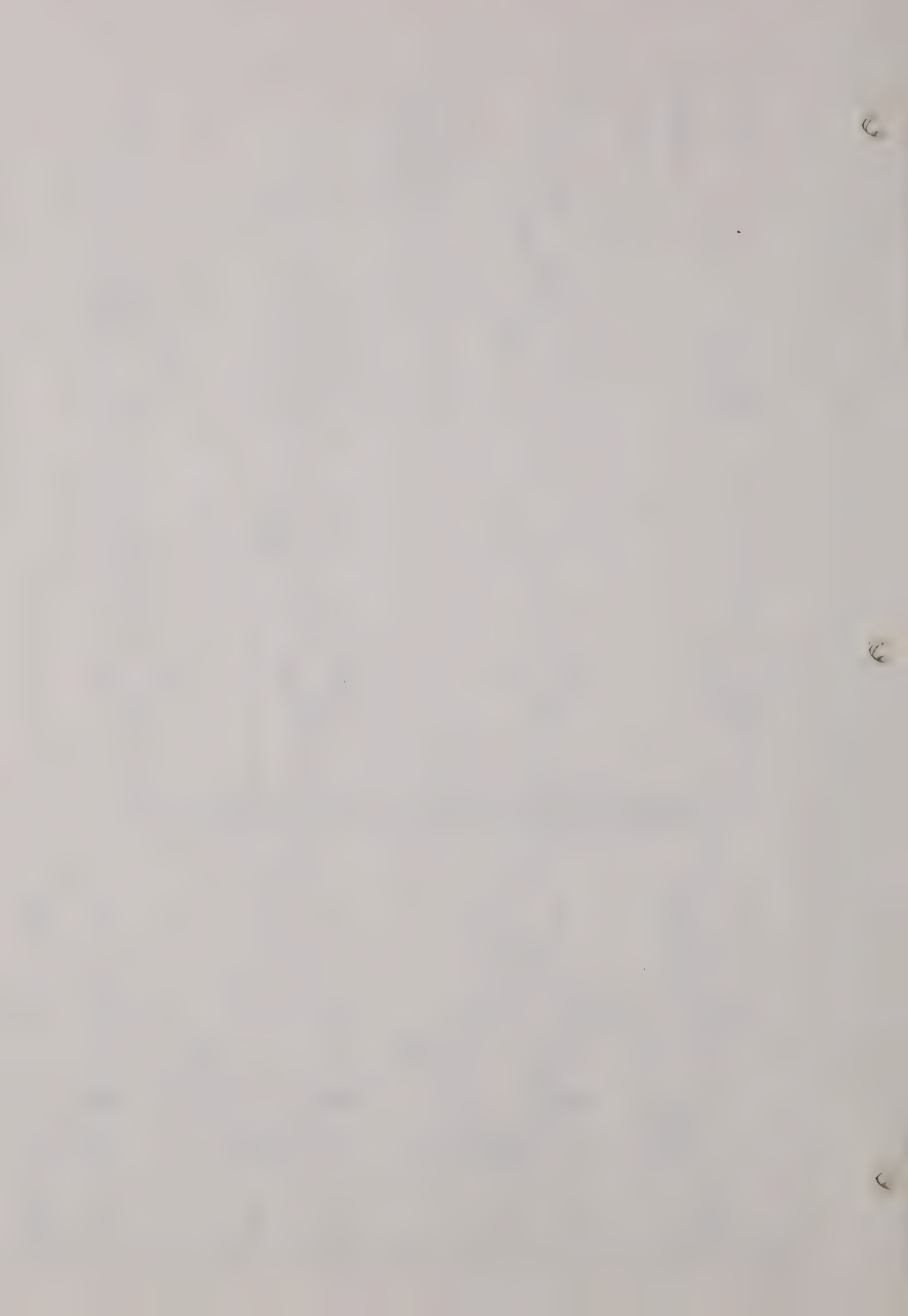
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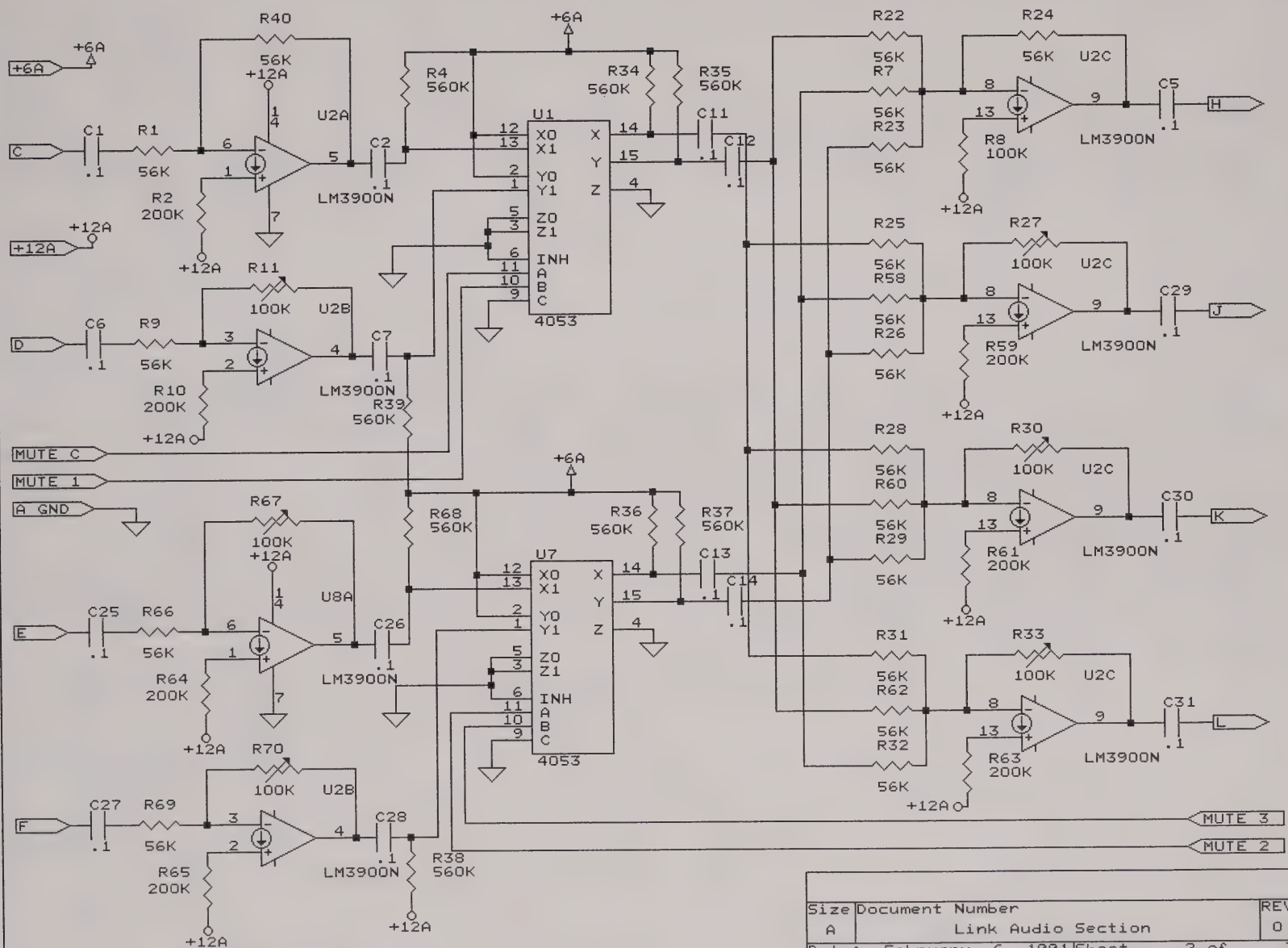
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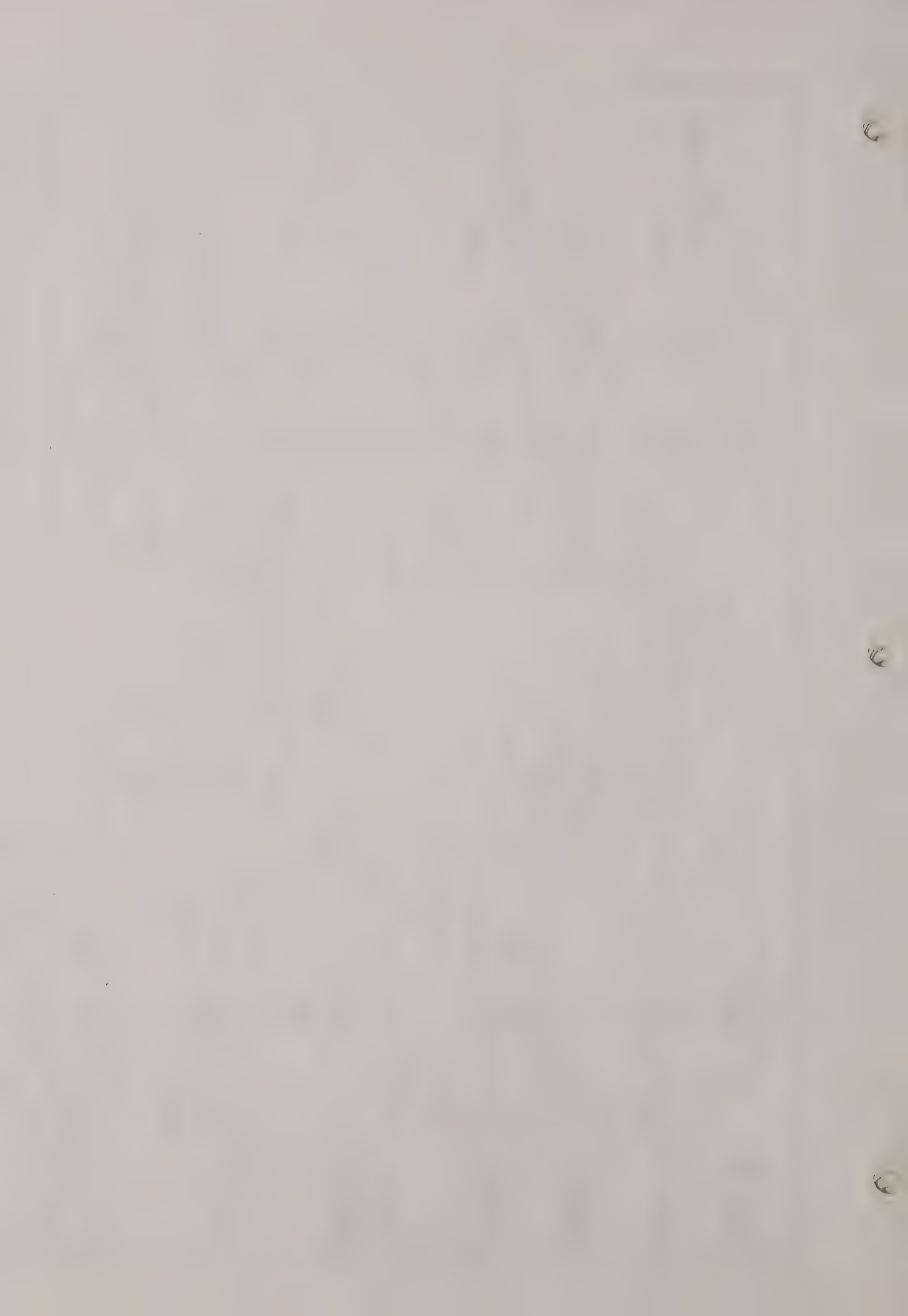
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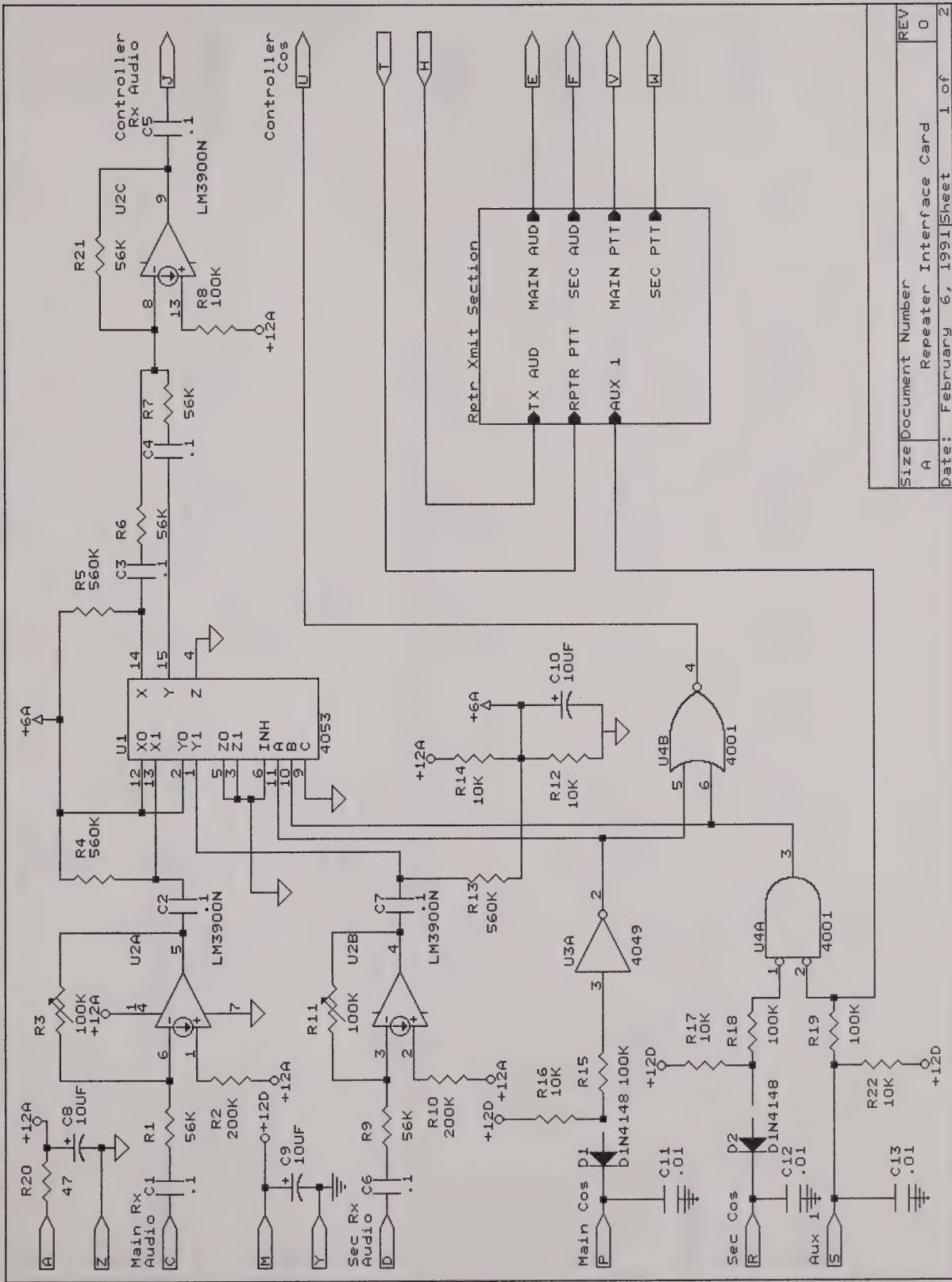


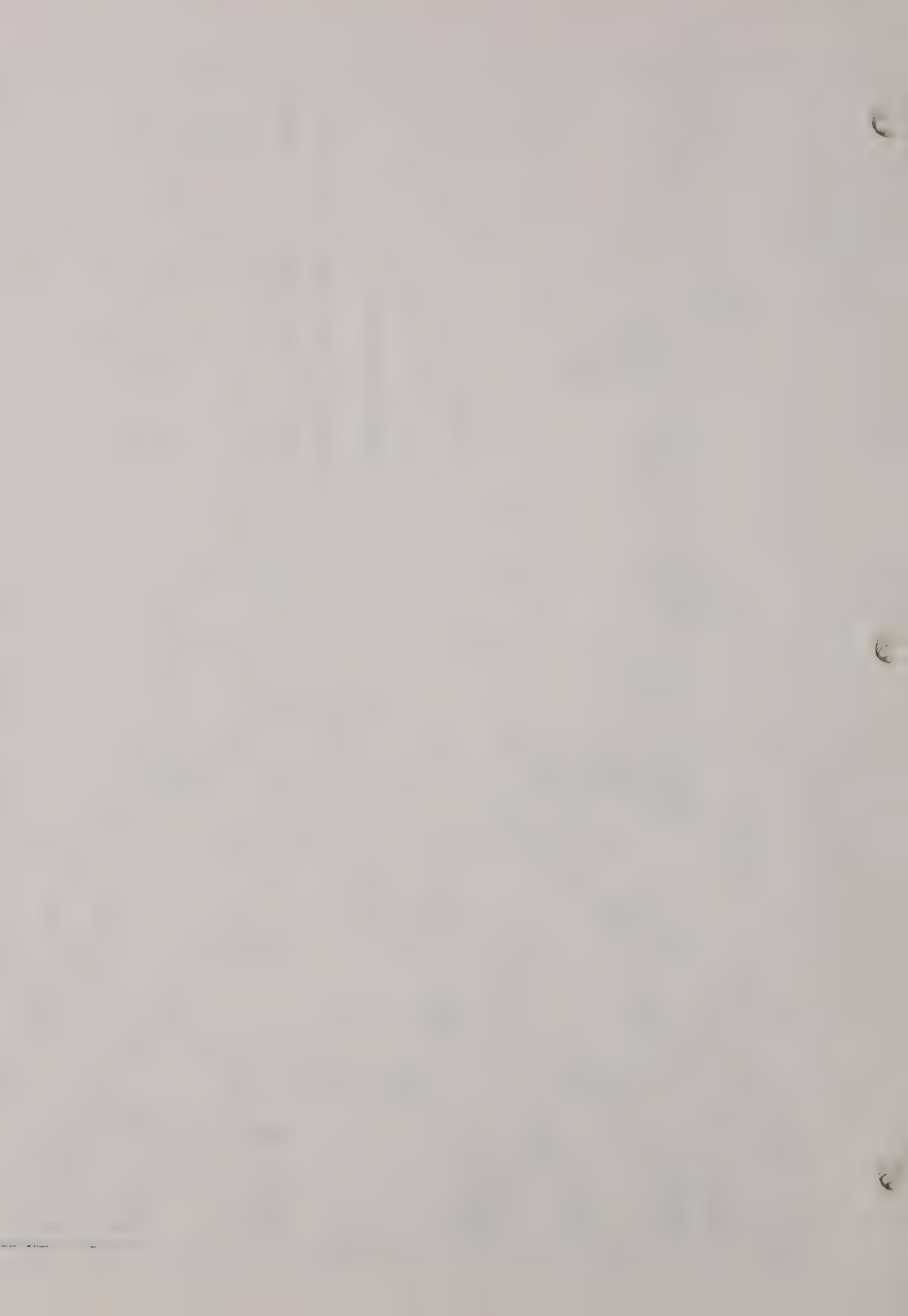


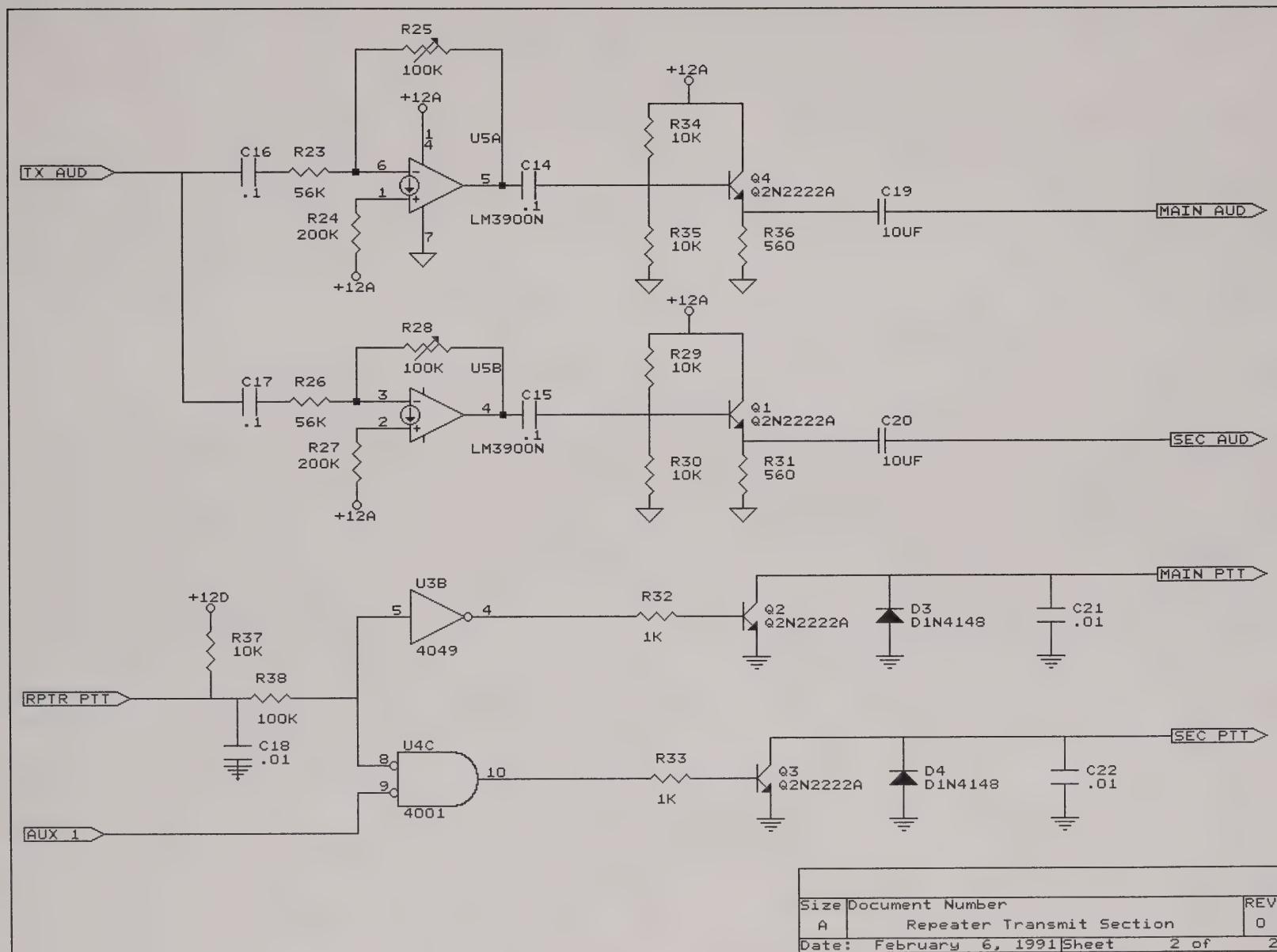












SERIES UDN-2980A HIGH-VOLTAGE, HIGH-CURRENT SOURCE DRIVERS

FEATURES

- TTL, DTL, PMOS, or CMOS Compatible Inputs
- 500 mA Output Source Current Capability
- Transient-Protected Outputs
- Output Breakdown Voltage to 80 V

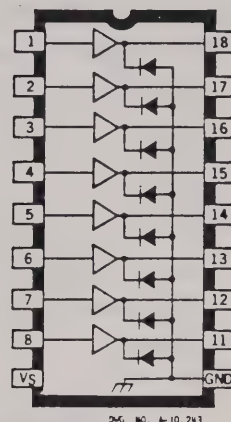
RECOMMENDED for applications requiring separate logic and load grounds, load supply voltage to +80 V, and load currents to 500 mA, Series UDN-2980A source drivers are used as interfaces between standard low-power digital logic and relays, solenoids, stepping motors, and LEDs.

Under normal operating conditions, these devices will sustain 120 mA continuously for each of the eight outputs at an ambient temperature of +50°C and a supply of +15 V. All devices in this series incorporate input current limiting resistors and output transient suppression diodes.

Type UDN-2981A and UDN-2983A drivers are for use with +5 V logic systems — TTL, Schottky TTL, DTL, and 5 V CMOS. Type UDN-2982A and UDN-2984A drivers are intended for MOS interface (PMOS and CMOS) operating from supply voltages

of 6 to 16 V. Types UDN-2981A and UDN-2982A will sustain a maximum output OFF voltage of +50 V, while Types UDN-2983A and UDN-2984A will sustain an output voltage of +80 V. In all cases, the output is switched ON by an active high input level.

Series UDN-2980A high-voltage, high-current source drivers are supplied in 18-lead dual in-line packages. On special order, hermetically-sealed versions of these devices (with reduced package power dissipation capability) can also be furnished.

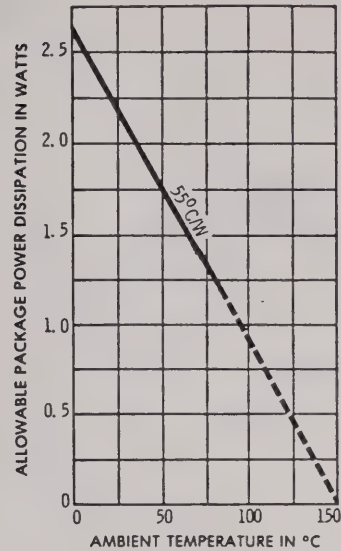
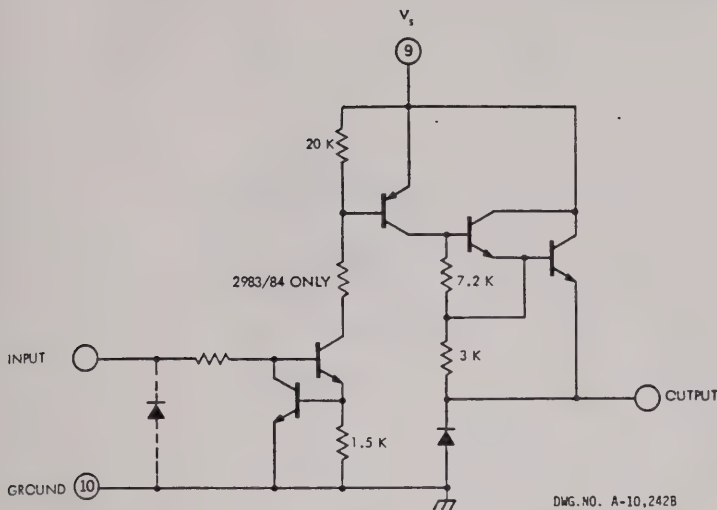


ABSOLUTE MAXIMUM RATINGS at 25°C Free-Air Temperature

Output Voltage Range, V_{CE} (UDN-2981A & UDN-2982A)	+5 V to +50 V
(UDN-2983A & UDN-2984A)	+35 V to +80 V
Input Voltage, V_{IN} (UDN-2981A & UDN-2983A)	+15 V
(UDN-2982A & UDN-2984A)	+30 V
Output Current, I_{OUT}	—500 mA
Power Dissipation, P_D (any one driver)	1.1 W
(total package)	2.2 W*
Operating Temperature Range, T_A	—20°C to +85°C
Storage Temperature Range, T_S	—55°C to +150°C

*Derate at the rate of 18 mW/°C above +25°C.

ONE OF EIGHT DRIVERS

POWER DISSIPATION
AS A FUNCTION OF AMBIENT TEMPERATURE

Dwg. No. A-11,112A

ELECTRICAL CHARACTERISTICS at $T_A = +25^\circ\text{C}$ (unless otherwise specified)

Characteristic	Symbol	Applicable Devices	Test Conditions	Test Fig.	Limit			
					Min.	Typ.	Max.	Units
Output Leakage Current	I_{CEX}	UDN-2981.82A	$V_{IN} = 0.4 \text{ V}^*$, $V_S = 50 \text{ V}$, $T_A = +70^\circ\text{C}$	1	—	—	200	μA
		UDN-2983.84A	$V_{IN} = 0.4 \text{ V}^*$, $V_S = 80 \text{ V}$, $T_A = +70^\circ\text{C}$	1	—	—	200	μA
Collector-Emitter Saturation Voltage	$V_{CE(SAT)}$	All	$V_{IN} = 2.4 \text{ V}$, $I_{OUT} = -100 \text{ mA}$	2	—	1.6	1.8	V
			$V_{IN} = 2.4 \text{ V}$, $I_{OUT} = -225 \text{ mA}$	2	—	1.7	1.9	V
			$V_{IN} = 2.4 \text{ V}$, $I_{OUT} = -350 \text{ mA}$	2	—	1.8	2.0	V
Input Current	$I_{IN(ON)}$	UDN-2981.83A	$V_{IN} = 2.4 \text{ V}$	3	—	140	200	μA
			$V_{IN} = 3.85 \text{ V}$	3	—	310	450	μA
		UDN-2982/84A	$V_{IN} = 2.4 \text{ V}$	3	—	140	200	μA
			$V_{IN} = 12 \text{ V}$	3	—	1.25	1.93	mA
Output Source Current	I_{OUT}	UDN-2981/83A	$V_{IN} = 2.4 \text{ V}$, $V_{CE} = 2.0 \text{ V}$	2	-350	—	—	mA
		UDN-2982/84A	$V_{IN} = 2.4 \text{ V}$, $V_{CE} = 2.0 \text{ V}$	2	-350	—	—	mA
Supply Current (Outputs Open)	I_S	UDN-2981.82A	$V_{IN} = 2.4 \text{ V}^*$, $V_S = 50 \text{ V}$	4	—	—	10	mA
		UDN-2983.84A	$V_{IN} = 2.4 \text{ V}^*$, $V_S = 80 \text{ V}$	4	—	—	10	mA
Clamp Diode Leakage Current	I_R	UDN-2981.82A	$V_R = 50 \text{ V}$, $V_{IN} = 0.4 \text{ V}^*$	5	—	—	50	μA
		UDN-2983.84A	$V_R = 80 \text{ V}$, $V_{IN} = 0.4 \text{ V}^*$	5	—	—	50	μA
Clamp Diode Forward Voltage	V_F	All	$I_F = 350 \text{ mA}$	6	—	1.5	2.0	V
Turn-On Delay	t_{ON}	All	$0.5 E_{IN}$ to $0.5 E_{OUT}$, $R_L = 100\Omega$, $V_S = 35 \text{ V}$	—	—	1.0	2.0	μs
Turn-Off Delay	t_{OFF}	All	$0.5 E_{IN}$ to $0.5 E_{OUT}$, $R_L = 100\Omega$, $V_S = 35 \text{ V}$	—	—	5.0	10	μs

*All Inputs Simultaneously

TEST FIGURES

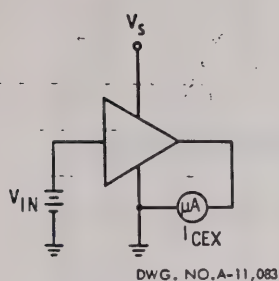


Figure 1

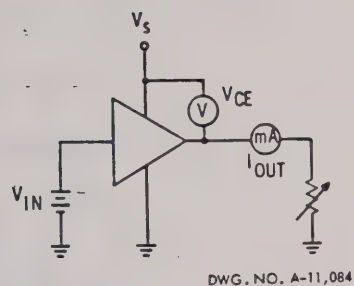


Figure 2

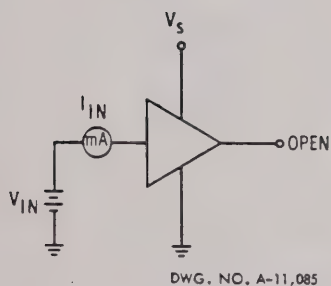


Figure 3

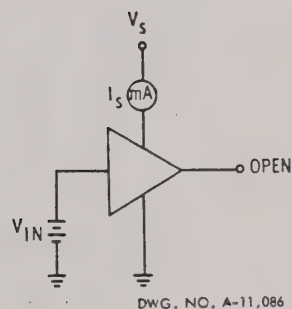


Figure 4

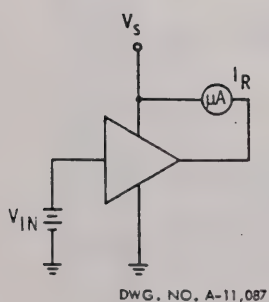


Figure 5

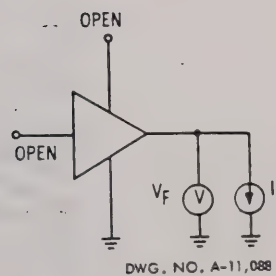
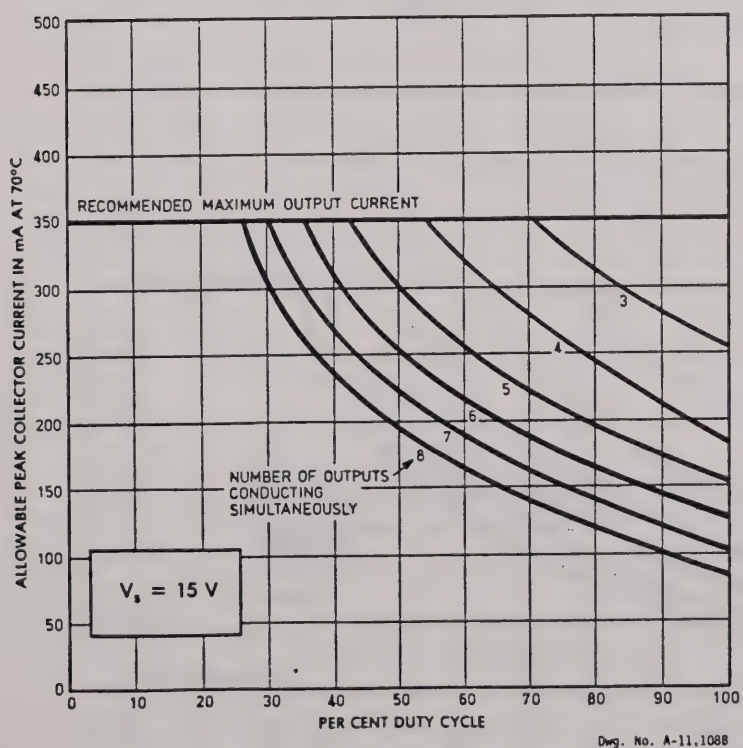
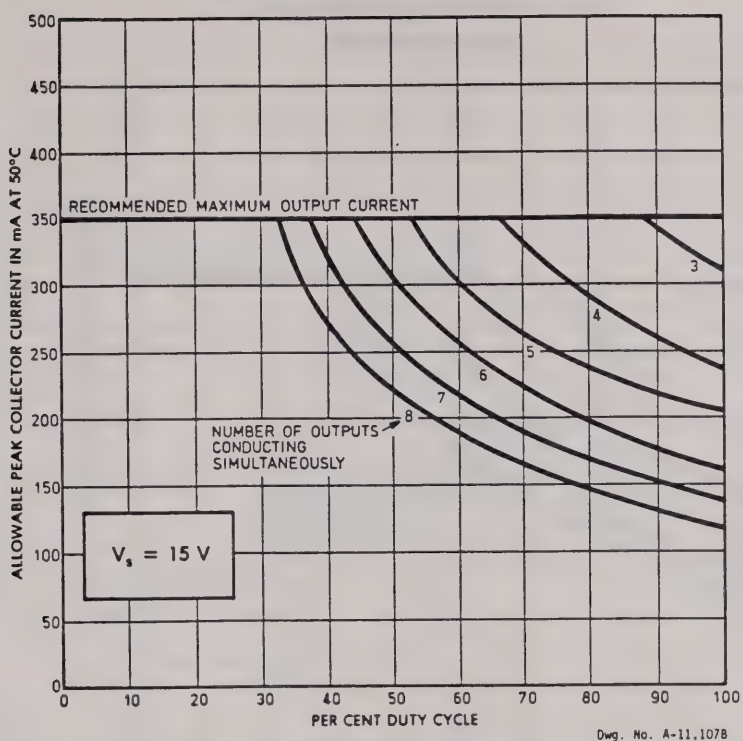
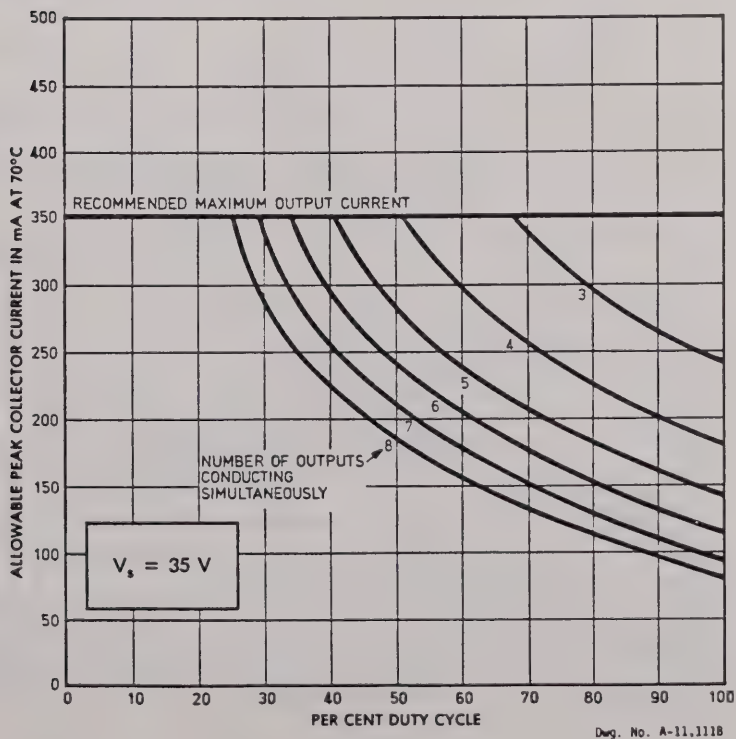
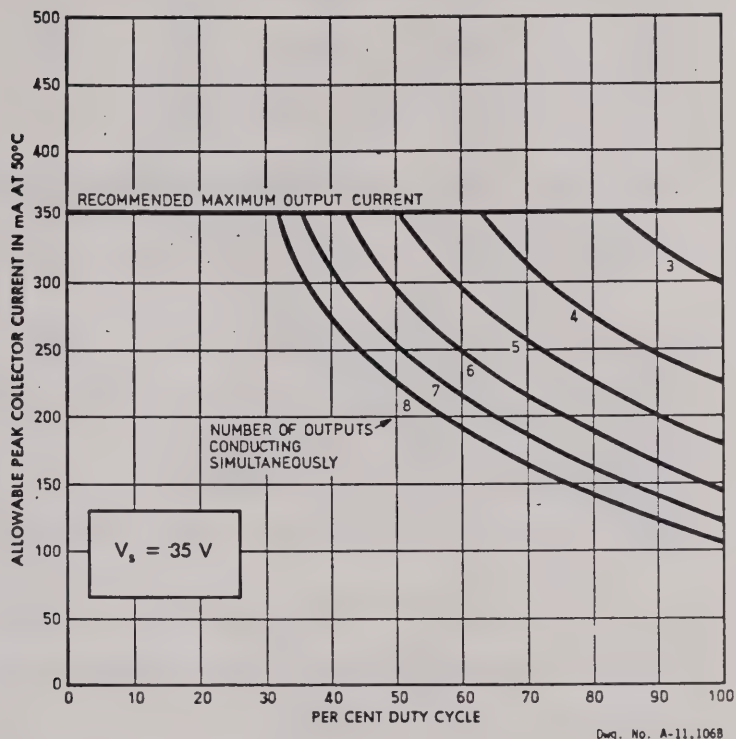


Figure 6

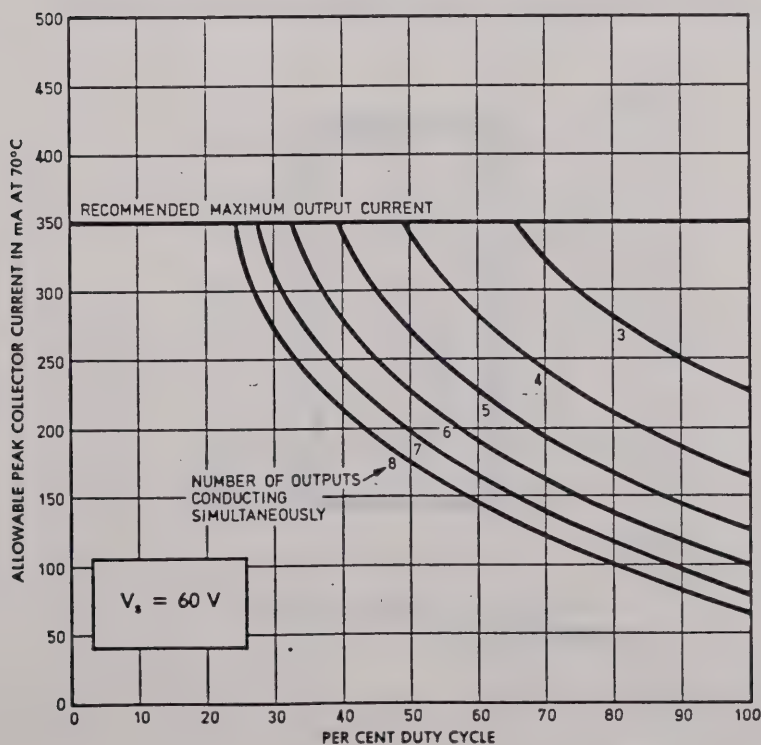
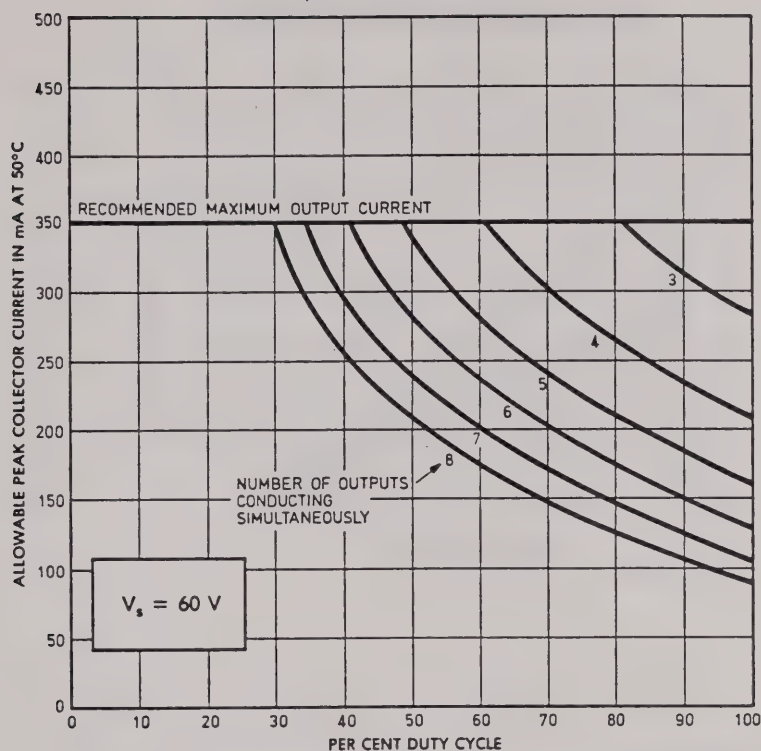
ALLOWABLE PEAK COLLECTOR CURRENT
AS A FUNCTION OF DUTY CYCLE
TYPE UDN-2981A/82A



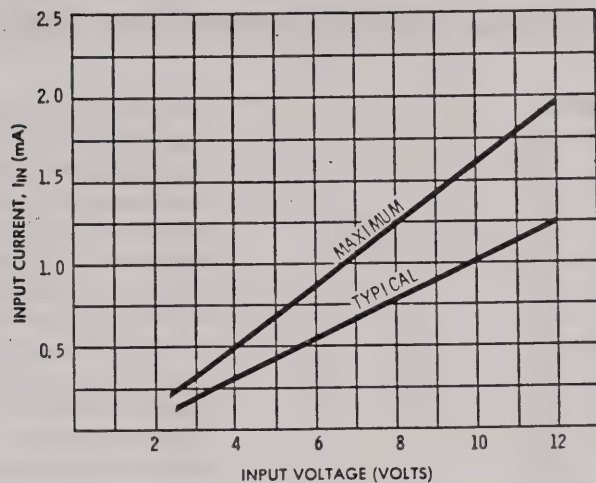
ALLOWABLE PEAK COLLECTOR CURRENT
AS A FUNCTION OF DUTY CYCLE
SERIES UDN-2980A



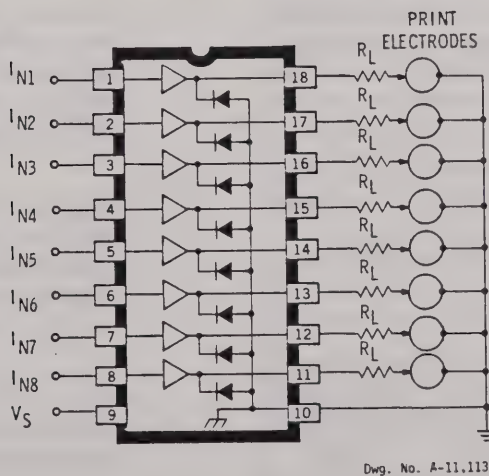
ALLOWABLE PEAK COLLECTOR CURRENT
AS A FUNCTION OF DUTY CYCLE
TYPES UDN-2983A/84A



INPUT CURRENT AS A FUNCTION OF INPUT VOLTAGE



TYPICAL ELECTROSENSITIVE PRINTER APPLICATION



TYPICAL VALUES: $V_S = 50\text{ V}$
 $I_{OUT} = 200\text{-}300\text{ mA}$

SERIES ULN-2800A

HIGH-VOLTAGE, HIGH-CURRENT

DARLINGTON TRANSISTOR ARRAYS

IDEALLY SUITED for interfacing between low-level digital logic circuitry and high-power peripheral loads, the Series ULN-2800A high-voltage, high-current Darlington transistor arrays feature peak load current ratings of 600 mA (Series ULN-2800A and ULN-2820A) or 750 mA (Series ULN-2810A) for each of the eight drivers in each device. Under the proper conditions, high-power loads of up to 4 A at 50V (200 W at 23% duty cycle) or 3.2 A at 95 V (304 W at 33% duty cycle) can be controlled. Typical loads include relays, solenoids, stepping motors, multiplexed LED and incandescent displays, and heaters. All devices feature open collector outputs and integral diodes for inductive load transient suppression.

The Series ULN-2801A devices are general purpose arrays which may be used with standard bipolar digital logic using external current limiting, or with most PMOS or CMOS directly. All are pinned with outputs opposite inputs to facilitate ease of circuit board layout and are priced to compete directly with discrete transistor alternatives.

The Series ULN-2802A was specifically designed for use with 14 to 25 V PMOS devices. Each input has a Zener diode and resistor in series to limit the input current to a safe value in that application. The Zener diode also means excellent noise immunity for these devices.

The Series ULN-2803A has a 2.7 k Ω series base resistor to each Darlington pair, and thus allows operation directly with TTL or CMOS operating at a supply voltage of 5 V. These devices will handle numerous interface needs – particularly those beyond the capabilities of standard logic buffers.

The Series ULN-2804A features a 10.5 k Ω series input resistor to permit their operation directly from CMOS or PMOS outputs utilizing supply voltages of 6 to 15 V. The required input current is below that of the Series ULN-2803A while the required input voltage is less than that required by the Series ULN-2802A.

The Series ULN-2805A is especially designed for use with standard and Schottky TTL where higher output currents are required and loading of the logic

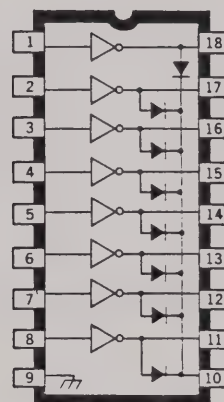


FIG. 10. A-10.322

output is not a concern. These devices will sink a minimum of 350 mA when driven from a "totem pole" logic output.

The Series ULN-2800A is the standard high-voltage, high-current Darlington array. The output transistors are capable of sinking 500mA and will withstand at least 50 V in the OFF state. Outputs may be paralleled for higher load current capability. The Series ULN-2810A devices are similar except that they will sink 600mA. The Series ULN-2820A will withstand 95 V in the OFF state.

All Series ULN-2800A Darlington arrays are furnished in an 18-pin dual in-line plastic package.

Device Type Number Designation

$V_{CE(MAX)} =$ $I_{C(MAX)} =$	50 V 500 mA	50 V 600 mA	95 V 500 mA
	Type Number		
General Purpose PMOS, CMOS	ULN-2801A	ULN-2811A	ULN-2821A
14 - 25 V PMOS	ULN-2802A	ULN-2812A	ULN-2822A
5 V TTL, CMOS	ULN-2803A	ULN-2813A	ULN-2823A
6 - 15 V CMOS, PMOS	ULN-2804A	ULN-2814A	ULN-2824A
High Output TTL	ULN-2805A	ULN-2815A	ULN-2825A

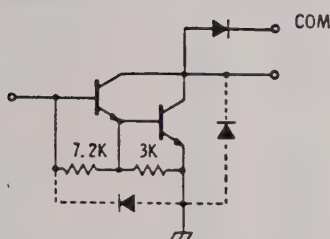
**ABSOLUTE MAXIMUM RATINGS at 25°C Free-Air Temperature
for any one Darlington pair (unless otherwise noted)**

Output Voltage, V_{CE} (Series ULN-2800, 2810A)	50 V
(Series ULN-2820A)	95 V
Input Voltage, V_{IN} (Series ULN-2802, 2803, 2804A)	30 V
(Series ULN-2805A)	15 V
Continuous Collector Current, I_C (Series ULN-2800, 2820A)	500 mA
(Series ULN-2810A)	600 mA
Continuous Base Current, I_B	25 mA
Power Dissipation, P_D (one Darlington pair)	1.0 W
(total package)	2.25 W*
Operating Ambient Temperature Range, T_A	-20°C to +85°C
Storage Temperature Range, T_S	-55°C to +150°C

*Derate at the rate of 18.18mW/°C above 25°C.

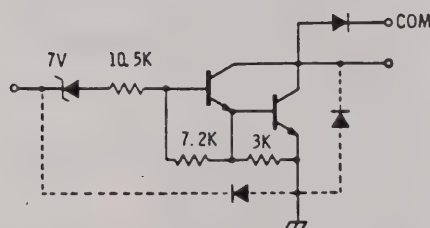
Under normal operating conditions, these devices will sustain 350 mA per output with $V_{CE(SAT)} = 1.6$ V at 50°C with a pulse width of 20 ms and a duty cycle of 40%.

PARTIAL SCHEMATICS



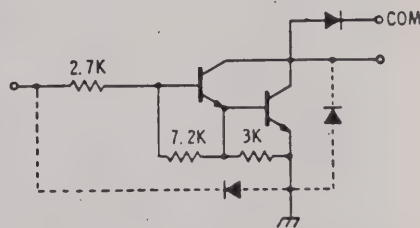
DWG. NO. A-9535

Series ULN-2801A
(each driver)



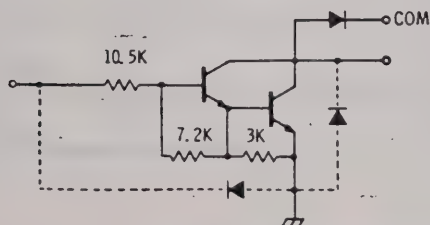
DWG. NO. A-9650

Series ULN-2802A
(each driver)



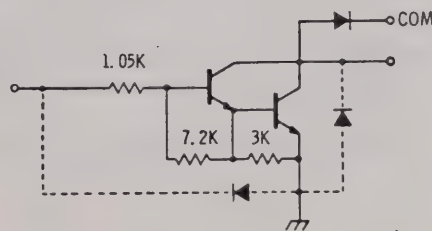
DWG. NO. A-9651

Series ULN-2803A
(each driver)



DWG. NO. A-9898A

Series ULN-2804A
(each driver)



1-1 G. NO. A-10-228

Series ULN-2805A
(each driver)

SERIES ULN-2800A

ELECTRICAL CHARACTERISTICS at 25°C (unless otherwise noted)

Characteristic	Symbol	Test Fig.	Applicable Devices	Test Conditions	Limits		
					Min.	Typ.	Max. Units
Output Leakage Current	I_{CEX}	1A	All	$V_{CE} = 50 \text{ V}, T_A = 25^\circ\text{C}$	—	—	50 μA
				$V_{CE} = 50 \text{ V}, T_A = 70^\circ\text{C}$	—	—	100 μA
		1B	ULN-2802A	$V_{CE} = 50 \text{ V}, T_A = 70^\circ\text{C}, V_{IN} = 6.0 \text{ V}$	—	—	500 μA
			ULN-2804A	$V_{CE} = 50 \text{ V}, T_A = 70^\circ\text{C}, V_{IN} = 1.0 \text{ V}$	—	—	500 μA
Collector-Emitter Saturation Voltage	$V_{CE(SAT)}$	2	All	$I_C = 100 \text{ mA}, I_B = 250 \mu\text{A}$	—	0.9	1.1 V
				$I_C = 200 \text{ mA}, I_B = 350 \mu\text{A}$	—	1.1	1.3 V
				$I_C = 350 \text{ mA}, I_B = 500 \mu\text{A}$	—	1.3	1.6 V
Input Current	$I_{IN(ON)}$	3	ULN-2802A	$V_{IN} = 17 \text{ V}$	—	0.82	1.25 mA
			ULN-2803A	$V_{IN} = 3.85 \text{ V}$	—	0.93	1.35 mA
			ULN-2804A	$V_{IN} = 5.0 \text{ V}$	—	0.35	0.5 mA
				$V_{IN} = 12 \text{ V}$	—	1.0	1.45 mA
	$I_{IN(OFF)}$	4	All	$I_C = 500 \mu\text{A}, T_A = 70^\circ\text{C}$	—	1.5	2.4 mA
Input Voltage	$V_{IN(ON)}$	5	ULN-2802A	$V_{CE} = 2.0 \text{ V}, I_C = 300 \text{ mA}$	—	—	13 V
				$V_{CE} = 2.0 \text{ V}, I_C = 200 \text{ mA}$	—	—	2.4 V
			ULN-2803A	$V_{CE} = 2.0 \text{ V}, I_C = 250 \text{ mA}$	—	—	2.7 V
				$V_{CE} = 2.0 \text{ V}, I_C = 300 \text{ mA}$	—	—	3.0 V
			ULN-2804A	$V_{CE} = 2.0 \text{ V}, I_C = 125 \text{ mA}$	—	—	5.0 V
				$V_{CE} = 2.0 \text{ V}, I_C = 200 \text{ mA}$	—	—	6.0 V
				$V_{CE} = 2.0 \text{ V}, I_C = 275 \text{ mA}$	—	—	7.0 V
				$V_{CE} = 2.0 \text{ V}, I_C = 350 \text{ mA}$	—	—	8.0 V
D-C Forward Current Transfer Ratio	h_{FE}	2	ULN-2801A	$V_{CE} = 2.0 \text{ V}, I_C = 350 \text{ mA}$	1000	—	—
			All		—	15	25 pF
Input Capacitance	C_{IN}	—	All		—	15	25 pF
Turn-On Delay	t_{ON}	—	All	$0.5 E_{in}$ to $0.5 E_{out}$	—	0.25	1.0 μs
Turn-Off Delay	t_{OFF}	—	All	$0.5 E_{in}$ to $0.5 E_{out}$	—	0.25	1.0 μs
Clamp Diode Leakage Current	I_R	6	All	$V_R = 50 \text{ V}, T_A = 25^\circ\text{C}$	—	—	50 μA
				$V_R = 50 \text{ V}, T_A = 70^\circ\text{C}$	—	—	100 μA
Clamp Diode Forward Voltage	V_F	7	All	$I_F = 350 \text{ mA}$	—	1.7	2.0 V

Series ULN-2800A and ULN-2810A devices are also available (with reduced package power capability) in industrial-grade hermetic packages. To order, change the last letter of the part number from 'A' to 'R'. Note that the high-voltage devices ($BV_{CE} \geq 95 \text{ V}$) are not presently available with this packaging option.

SERIES ULN-2810A

ELECTRICAL CHARACTERISTICS at 25°C (unless otherwise noted)

Characteristic	Symbol	Test Fig.	Applicable Devices	Test Conditions	Limits			
					Min.	Typ.	Max.	Units
Output Leakage Current	I_{CEX}	1A	All	$V_{CE} = 50 \text{ V}, T_A = 25^\circ\text{C}$	—	—	50	μA
				$V_{CE} = 50 \text{ V}, T_A = 70^\circ\text{C}$	—	—	100	μA
		1B	ULN-2812A	$V_{CE} = 50 \text{ V}, T_A = 70^\circ\text{C}, V_{IN} = 6.0 \text{ V}$	—	—	500	μA
			ULN-2814A	$V_{CE} = 50 \text{ V}, T_A = 70^\circ\text{C}, V_{IN} = 1.0 \text{ V}$	—	—	500	μA
Collector-Emitter Saturation Voltage	$V_{CE(SAT)}$	2	All	$I_C = 200 \text{ mA}, I_B = 350 \mu\text{A}$	—	1.1	1.3	V
				$I_C = 350 \text{ mA}, I_B = 500 \mu\text{A}$	—	1.3	1.6	V
				$I_C = 500 \text{ mA}, I_B = 600 \mu\text{A}$	—	1.7	1.9	V
Input Current	$I_{IN(ON)}$	3	ULN-2812A	$V_{IN} = 17 \text{ V}$	—	0.82	1.25	mA
			ULN-2813A	$V_{IN} = 3.85 \text{ V}$	—	0.93	1.35	mA
			ULN-2814A	$V_{IN} = 5.0 \text{ V}$	—	0.35	0.5	mA
				$V_{IN} = 12 \text{ V}$	—	1.0	1.45	mA
	$I_{IN(OFF)}$	4	All	$I_C = 500 \mu\text{A}, T_A = 70^\circ\text{C}$	50	65	—	μA
Input Voltage	$V_{IN(ON)}$	5	ULN-2812A	$V_{CE} = 2.0 \text{ V}, I_C = 500 \text{ mA}$	—	—	17	V
			ULN-2813A	$V_{CE} = 2.0 \text{ V}, I_C = 250 \text{ mA}$	—	—	2.7	V
				$V_{CE} = 2.0 \text{ V}, I_C = 300 \text{ mA}$	—	—	3.0	V
				$V_{CE} = 2.0 \text{ V}, I_C = 500 \text{ mA}$	—	—	3.5	V
			ULN-2814A	$V_{CE} = 2.0 \text{ V}, I_C = 275 \text{ mA}$	—	—	7.0	V
				$V_{CE} = 2.0 \text{ V}, I_C = 350 \text{ mA}$	—	—	8.0	V
				$V_{CE} = 2.0 \text{ V}, I_C = 500 \text{ mA}$	—	—	9.5	V
			ULN-2815A	$V_{CE} = 2.0 \text{ V}, I_C = 500 \text{ mA}$	—	—	2.6	V
D-C Forward Current Transfer Ratio	h_{FE}	2	ULN-2811A	$V_{CE} = 2.0 \text{ V}, I_C = 350 \text{ mA}$	1000	—	—	
				$V_{CE} = 2.0 \text{ V}, I_C = 500 \text{ mA}$	900	—	—	
Input Capacitance	C_{IN}	—	All		—	15	25	pF
Turn-On Delay	t_{ON}	—	All	$0.5 E_{in} \text{ to } 0.5 E_{out}$	—	0.25	1.0	μs
Turn-Off Delay	t_{OFF}	—	All	$0.5 E_{in} \text{ to } 0.5 E_{out}$	—	0.25	1.0	μs
Clamp Diode Leakage Current	I_R	6	All	$V_R = 50 \text{ V}, T_A = 25^\circ\text{C}$	—	—	50	μA
				$V_R = 50 \text{ V}, T_A = 70^\circ\text{C}$	—	—	100	μA
Clamp Diode Forward Voltage	V_F	7	All	$I_F = 350 \text{ mA}$	—	1.7	2.0	V
				$I_F = 500 \text{ mA}$	—	2.1	2.5	V

Series ULN-2800A and ULN-2810A devices are also available (with reduced package power capability) in industrial-grade hermetic packages. To order, change the last letter of the part number from 'A' to 'R'. Note that the high-voltage devices ($BV_{CE} \geq 95 \text{ V}$) are not presently available with this packaging option.

SERIES ULN-2820A

ELECTRICAL CHARACTERISTICS at 25°C (unless otherwise noted)

Characteristic	Symbol	Test Fig.	Applicable Devices	Test Conditions	Limits			
					Min.	Typ.	Max.	Units
Output Leakage Current	I_{CEX}	1A	All	$V_{CE} = 95\text{ V}, T_A = 25^\circ\text{C}$	—	—	50	μA
				$V_{CE} = 95\text{ V}, T_A = 70^\circ\text{C}$	—	—	100	μA
		1B	ULN-2822A	$V_{CE} = 95\text{ V}, T_A = 70^\circ\text{C}, V_{IN} = 6.0\text{ V}$	—	—	500	μA
			ULN-2824A	$V_{CE} = 95\text{ V}, T_A = 70^\circ\text{C}, V_{IN} = 1.0\text{ V}$	—	—	500	μA
Collector-Emitter Saturation Voltage	$V_{CE(SAT)}$	2	All	$I_C = 100\text{ mA}, I_B = 250\text{ }\mu\text{A}$	—	0.9	1.1	V
				$I_C = 200\text{ mA}, I_B = 350\text{ }\mu\text{A}$	—	1.1	1.3	V
				$I_C = 350\text{ mA}, I_B = 500\text{ }\mu\text{A}$	—	1.3	1.6	V
Input Current	$I_{IN(ON)}$	3	ULN-2822A	$V_{IN} = 17\text{ V}$	—	0.82	1.25	mA
			ULN-2823A	$V_{IN} = 3.85\text{ V}$	—	0.93	1.35	mA
			ULN-2824A	$V_{IN} = 5.0\text{ V}$	—	0.35	0.5	mA
				$V_{IN} = 12\text{ V}$	—	1.0	1.45	mA
			ULN-2825A	$V_{IN} = 3.0\text{ V}$	—	1.5	2.4	mA
	$I_{IN(OFF)}$	4	All	$I_C = 500\text{ }\mu\text{A}, T_A = 70^\circ\text{C}$	50	65	—	μA
Input Voltage	$V_{IN(ON)}$	5	ULN-2822A	$V_{CE} = 2.0\text{ V}, I_C = 300\text{ mA}$	—	—	13	V
			ULN-2823A	$V_{CE} = 2.0\text{ V}, I_C = 200\text{ mA}$	—	—	2.4	V
				$V_{CE} = 2.0\text{ V}, I_C = 250\text{ mA}$	—	—	2.7	V
				$V_{CE} = 2.0\text{ V}, I_C = 300\text{ mA}$	—	—	3.0	V
			ULN-2824A	$V_{CE} = 2.0\text{ V}, I_C = 125\text{ mA}$	—	—	5.0	V
				$V_{CE} = 2.0\text{ V}, I_C = 200\text{ mA}$	—	—	6.0	V
				$V_{CE} = 2.0\text{ V}, I_C = 275\text{ mA}$	—	—	7.0	V
				$V_{CE} = 2.0\text{ V}, I_C = 350\text{ mA}$	—	—	8.0	V
			ULN-2825A	$V_{CE} = 2.0\text{ V}, I_C = 350\text{ mA}$	—	—	2.4	V
D-C Forward Current Transfer Ratio	h_{FE}	2	ULN-2821A	$V_{CE} = 2.0\text{ V}, I_C = 350\text{ mA}$	1000	—	—	
Input Capacitance	C_{IN}	—	All		—	15	25	pF
Turn-On Delay	t_{ON}	—	All	$0.5 E_{in}$ to $0.5 E_{out}$	—	0.25	1.0	μs
Turn-Off Delay	t_{OFF}	—	All	$0.5 E_{in}$ to $0.5 E_{out}$	—	0.25	1.0	μs
Clamp Diode Leakage Current	I_R	6	All	$V_R = 95\text{ V}, T_A = 25^\circ\text{C}$	—	—	50	μA
				$V_R = 95\text{ V}, T_A = 70^\circ\text{C}$	—	—	100	μA
Clamp Diode Forward Voltage	V_F	7	All	$I_F = 350\text{ mA}$	—	1.7	2.0	V

TEST FIGURES

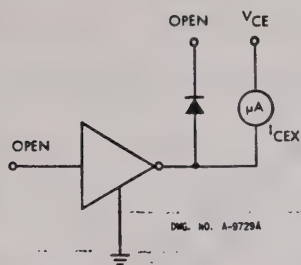


FIGURE 1A

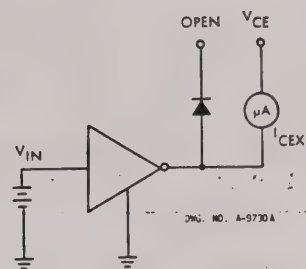


FIGURE 1B

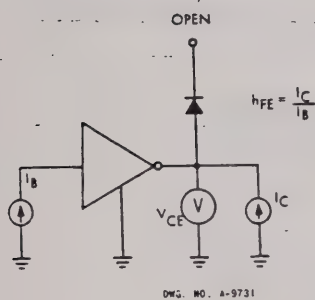


FIGURE 2

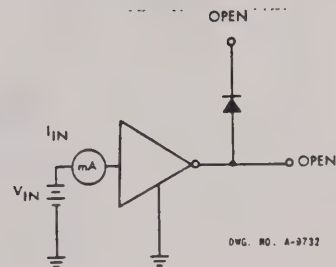


FIGURE 3

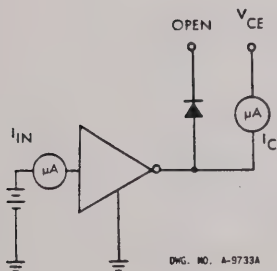


FIGURE 4

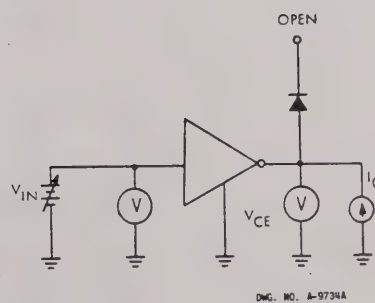


FIGURE 5

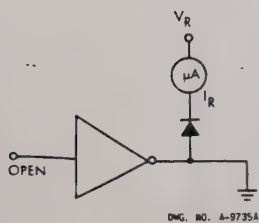


FIGURE 6

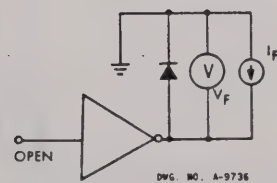
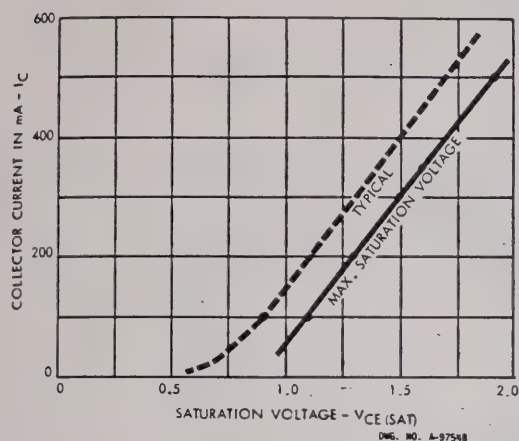
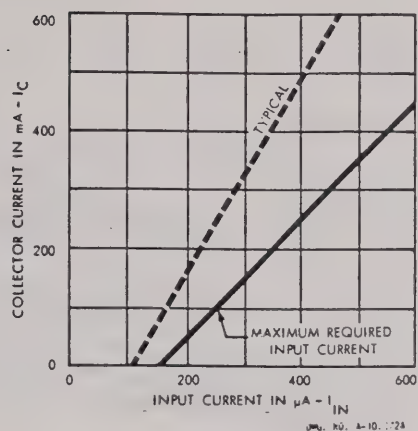


FIGURE 7

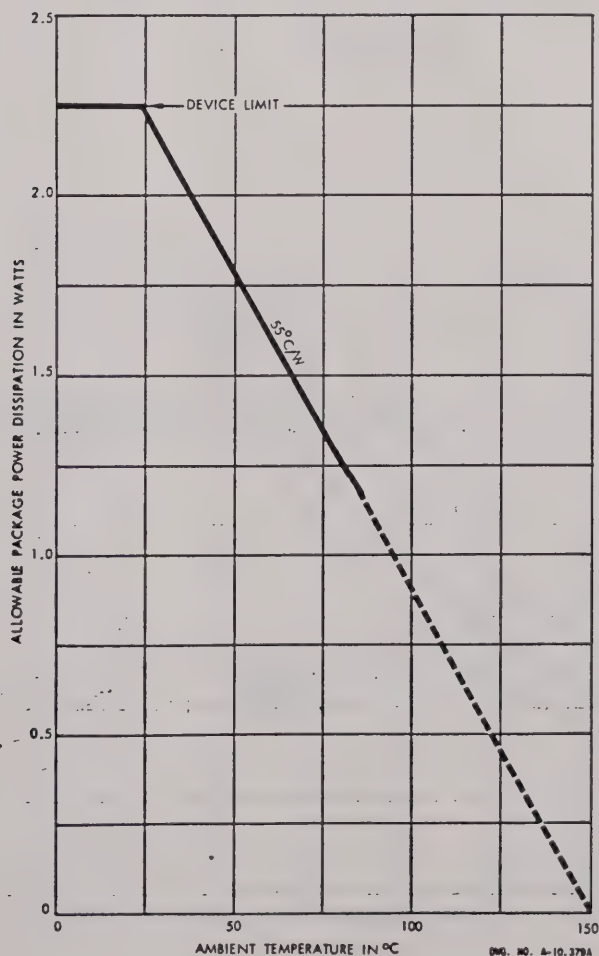
COLLECTOR CURRENT
AS A FUNCTION OF SATURATION VOLTAGE



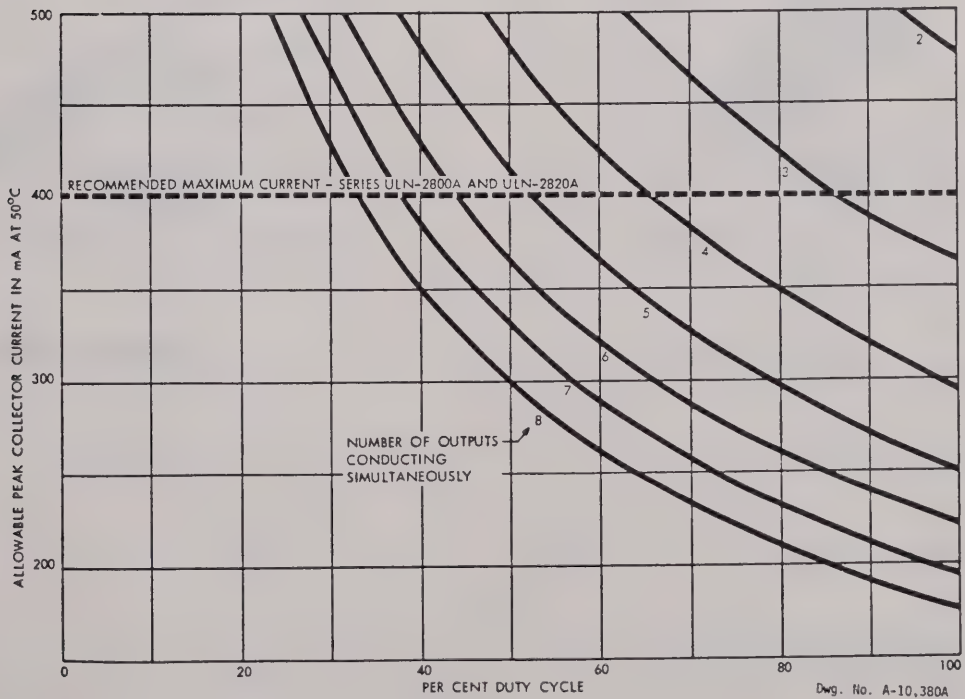
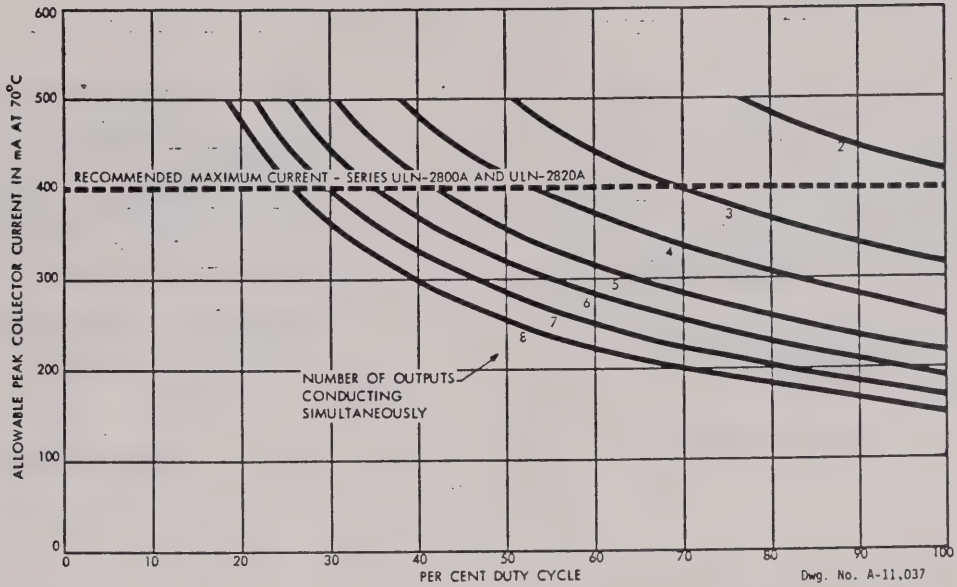
COLLECTOR CURRENT
AS A FUNCTION OF INPUT CURRENT



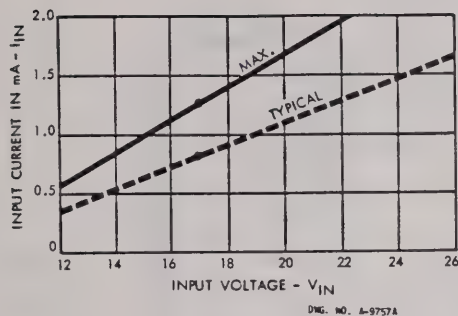
ALLOWABLE AVERAGE POWER DISSIPATION
AS A FUNCTION OF AMBIENT TEMPERATURE



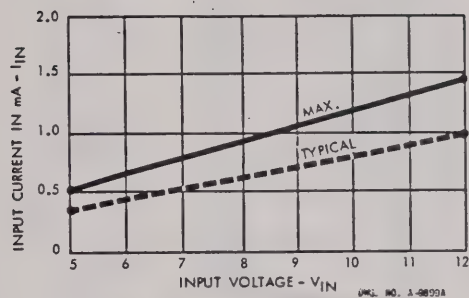
PEAK COLLECTOR CURRENT AS A FUNCTION OF DUTY CYCLE



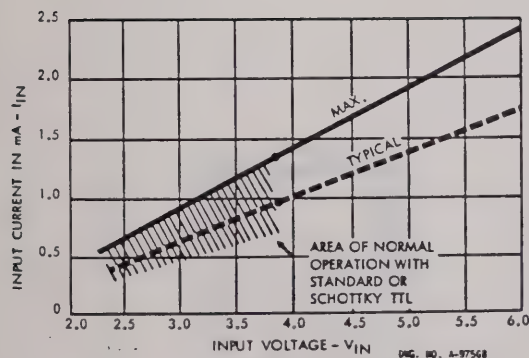
INPUT CURRENT AS A FUNCTION OF INPUT VOLTAGE



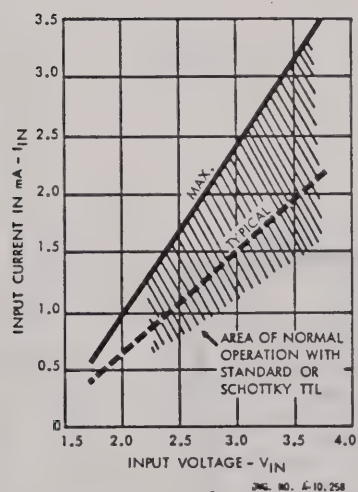
SERIES ULN-2802A



SERIES ULN-2804A

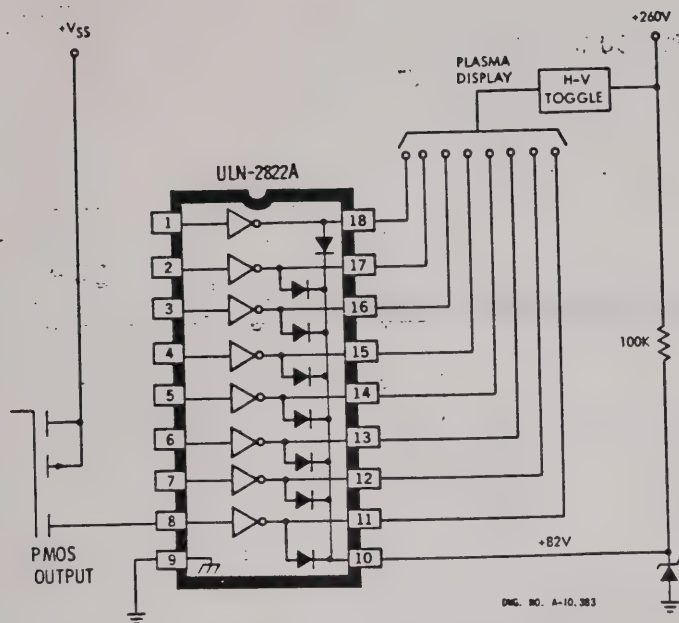


SERIES ULN-2803A

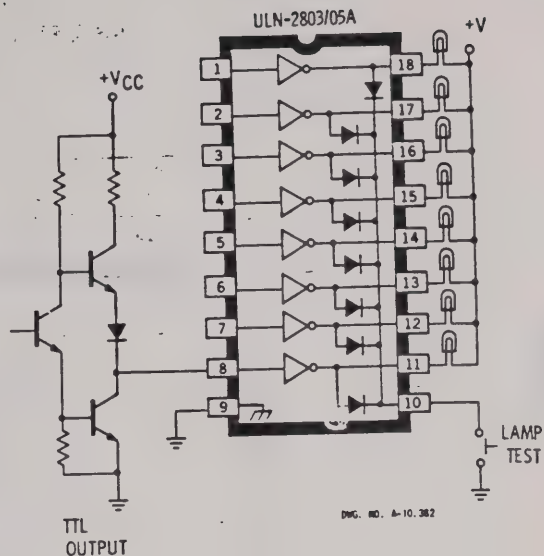


SERIES ULN-2805A

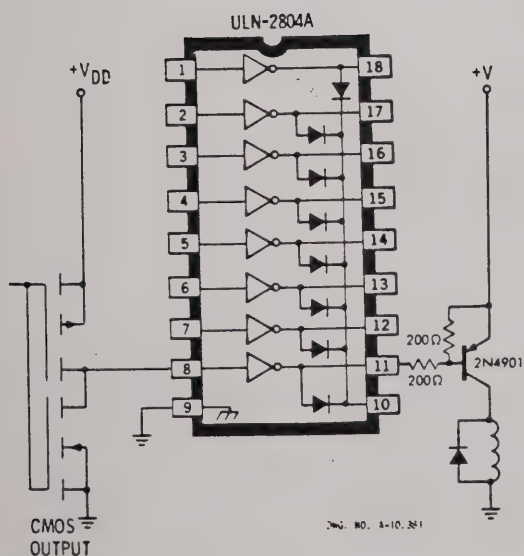
SERIES ULN-2800A HIGH-VOLTAGE, HIGH-CURRENT DARLINGTON TRANSISTOR ARRAYS



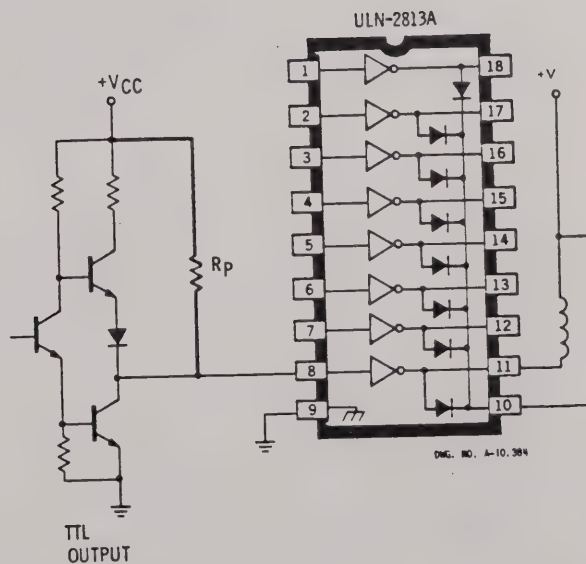
**OFF VOLTAGE BIAS FOR
HIGH-VOLTAGE LOADS**



TTL TO LOAD

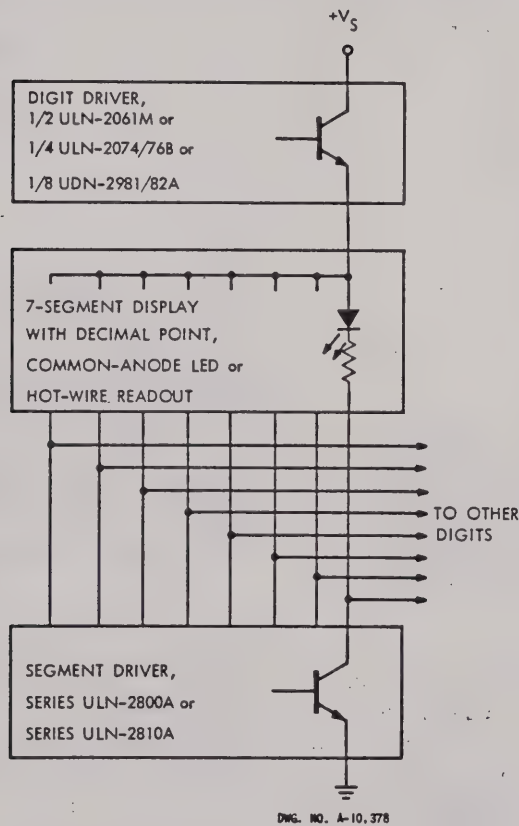


BUFFER FOR HIGHER CURRENT LOADS



**USE OF PULL-UP RESISTORS
TO INCREASE DRIVE CURRENT**

TYPICAL DISPLAY INTERFACE



UDN 2981 A PNP DAR
ULN 2803 A NPN DAR

SERIES ULS-2800H AND ULS-2800R HIGH-VOLTAGE, HIGH-CURRENT DARLINGTON TRANSISTOR ARRAYS

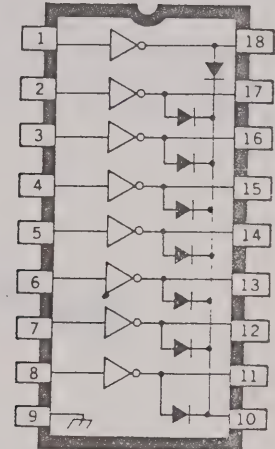
FEATURES

- TTL, DTL, PMOS, or CMOS Compatible Inputs
- Peak Output Current to 600 mA
- Transient Protected Outputs
- Side-Brazed Hermetic Package, or
- Cer-DIP Package
- High-Reliability Screening Available
- Wide Operating Temperature Ranges

DESIGNED for interfacing between low-level logic circuitry and high-power loads, the Series ULS-2800H and ULS-2800R arrays consist of eight silicon NPN Darlington power drivers on a common monolithic substrate. The choice of five input characteristics, two output voltage ratings (50 or 95 V), two output current ratings (500 or 600 mA), and two package styles (suffix 'H' or 'R') allow the circuit designer to select the optimum device for any specific application.

Both hermetically sealed package styles are rated for operation over the temperature range of -55°C to $+125^{\circ}\text{C}$, recommending them for military and aerospace applications or commercial and industrial applications where severe environmental conditions may be encountered.

The appropriate specific part number for use in standard logic applications can be determined from the Device Type Number Designation chart. Note that the high-voltage devices ($\text{BV}_{\text{CE}} \geq 95 \text{ V}$) are available in the Series ULS-2800H only. All units feature open collector outputs and integral diodes for inductive load transient suppression.



D·U. NO. 4-00 327

All Series ULS-2800H Darlington power drivers are furnished in an 18-pin side-brazed dual in-line hermetic package that meets the processing and environmental requirements of Military Standard MIL-STD-883, Methods 5004 and 5005.

Device Type Number Designation

$V_{\text{CE(MAX)}} =$ $I_{\text{C(MAX)}} =$	50 V 500 mA	50 V 600 mA	95 V 500 mA
	Type Number		
General-Purpose PMOS, CMOS	ULS-2801R	ULS-2811R	ULS-2821R
	ULS-2801H	ULS-2811H	
14-25 V PMOS	ULS-2802R	ULS-2812R	ULS-2822R
	ULS-2802H	ULS-2812H	
5 V TTL, CMOS	ULS-2803R	ULS-2813R	ULS-2823R
	ULS-2803H	ULS-2813H	
6-15 V CMOS, PMOS	ULS-2804R	ULS-2814R	ULS-2824R
	ULS-2804H	ULS-2814H	
High-Output TTL	ULS-2805R	ULS-2815R	ULS-2825R
	ULS-2805H	ULS-2815H	



EIGHT DARLINGTON ARRAYS

- EIGHT DARLINGTONS WITH COMMON EMITTERS
- OUTPUT CURRENT TO 500 mA
- OUTPUT VOLTAGE TO 50 V
- INTEGRAL SUPPRESSION DIODES
- VERSIONS FOR ALL POPULAR LOGIC FAMILIES
- OUTPUT CAN BE PARALLELED
- INPUTS PINNED OPPOSITE OUTPUTS TO SIMPLIFY BOARD LAYOUT

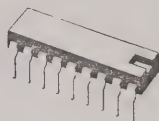
the ULN2804A has a 10.5 K Ω input resistor for 6-15 V CMOS and the ULN2805A is designed to sink a minimum of 350 mA for standard and Schottky TTL where higher output current is required.

All types are supplied in a 18-lead plastic DIP with a copper lead from and feature the convenient input-opposite-output pinout to simplify board layout.

DESCRIPTION

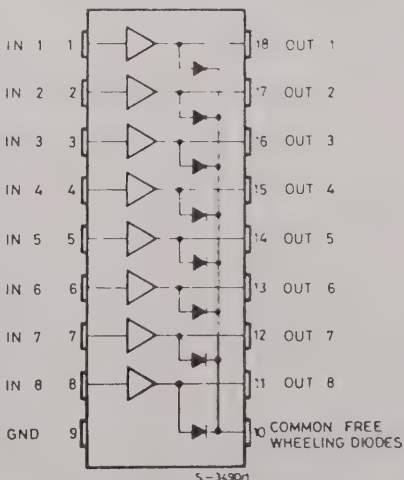
The ULN2801A-ULN2805A each contain eight darlington transistors with common emitters and integral suppression diodes for inductive loads. Each darlington features a peak load current rating of 600 mA (500 mA continuous) and can withstand at least 50 V in the off state. Outputs may be paralleled for higher current capability.

Five versions are available to simplify interfacing to standard logic families : the ULN2801A is designed for general purpose applications with a current limit resistor ; the ULN2802A has a 10.5 K Ω input resistor and zener for 14-25 V PMOS ; the ULN2803A has a 2.7 K Ω input resistor for 5 V TTL and CMOS ;



DIP-18
(Plastic)

CONNECTION DIAGRAM (top view)

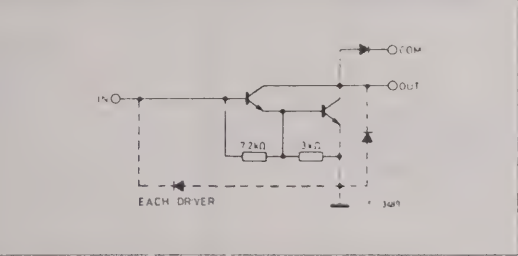


ABSOLUTE MAXIMUM RATINGS

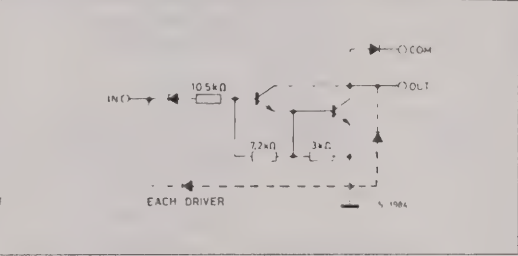
Symbol	Parameter	Value	Unit
V_o	Output Voltage	50	V
V_i	Input Voltage for ULN2802A, 2803A, 2804A for ULN2805A	30 15	V V
I_C	Continuous Collector Current	500	mA
I_B	Continuous Base Current	25	mA
P_{tot}	Power Dissipation (one Darlington pair) (total package)	1.0 2.25	W W
T_{amb}	Operating Ambient Temperature Range	- 20 to 85	°C
T_{stg}	Storage Temperature Range	- 55 to 150	°C

SCHEMATIC DIAGRAM AND ORDER CODES

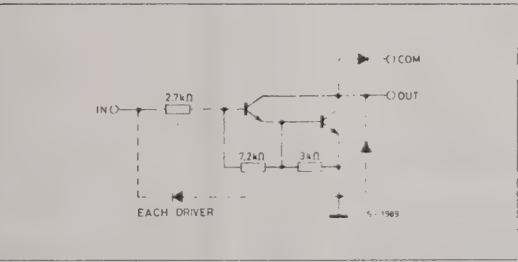
For ULN2801A (each driver for PMOS-CMOS)



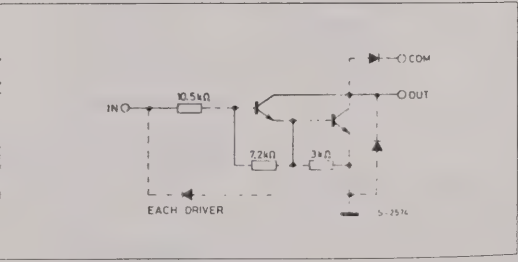
For ULN2802A (each driver for 14-15 V PMOS)



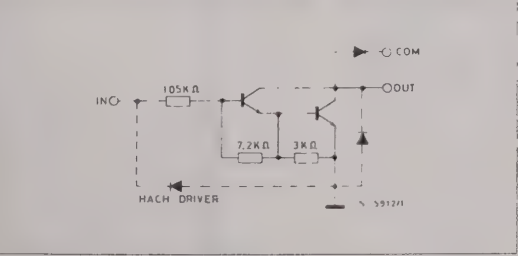
For ULN2803A (each driver for 5 V, TTL/CMOS)



For ULN2804A (each driver for 6-15 V CMOS/PMOS)



For ULN2805A (each driver for high out TTL)



THERMAL DATA

$R_{th\ j-amb}$	Thermal Resistance Junction-ambient	Max.	55	$^{\circ}\text{C/W}$
-----------------	-------------------------------------	------	----	----------------------

ELECTRICAL CHARACTERISTICS ($T_{amb} = 25^{\circ}\text{C}$ unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit	Fig.
I_{CEX}	Output Leakage Current	$V_{CE} = 50\text{ V}$ $T_{amb} = 70^{\circ}\text{C}$ $V_{CE} = 50\text{ V}$			50	μA	1a
		$T_{amb} = 70^{\circ}\text{C}$ for ULN2802A			100	μA	1a
		$V_{CE} = 50\text{ V}$ $V_i = 6\text{ V}$ for ULN2804A			500	μA	1b
		$V_{CE} = 50\text{ V}$ $V_i = 1\text{ V}$			500	μA	1b
$V_{CE(sat)}$	Collector-emitter Saturation Voltage	$I_C = 100\text{ mA}$ $I_B = 250\text{ }\mu\text{A}$	0.9	1.1	V		2
		$I_C = 200\text{ mA}$ $I_B = 350\text{ }\mu\text{A}$	1.1	1.3	V		
		$I_C = 350\text{ mA}$ $I_B = 500\text{ }\mu\text{A}$	1.3	1.6	V		
$I_{i(on)}$	Input Current	for ULN2802A $V_i = 17\text{ V}$	0.82	1.25	mA		3
		for ULN2803A $V_i = 3.85\text{ V}$	0.93	1.35	mA		
		for ULN2804A $V_i = 5\text{ V}$	0.35	0.5	mA		
		for ULN2805A $V_i = 12\text{ V}$	1	1.45	mA		
$I_{i(off)}$	Input Current	$T_{amb} = 70^{\circ}\text{C}$ $I_C = 500\text{ }\mu\text{A}$	50	65	μA		4
$V_{i(on)}$	Input Voltage	for ULN2802A $V_{CE} = 2\text{ V}$ $I_C = 300\text{ mA}$			13	V	5
		for ULN2803A $V_{CE} = 2\text{ V}$ $I_C = 200\text{ mA}$			2.4	V	
		$V_{CE} = 2\text{ V}$ $I_C = 250\text{ mA}$			2.7	V	
		$V_{CE} = 2\text{ V}$ $I_C = 300\text{ mA}$			3	V	
		for ULN2804A $V_{CE} = 2\text{ V}$ $I_C = 125\text{ mA}$			5	V	
		$V_{CE} = 2\text{ V}$ $I_C = 200\text{ mA}$			6	V	
		$V_{CE} = 2\text{ V}$ $I_C = 275\text{ mA}$			7	V	
		$V_{CE} = 2\text{ V}$ $I_C = 350\text{ mA}$			8	V	
		for ULN2805A $V_{CE} = 2\text{ V}$ $I_C = 350\text{ mA}$			2.4	V	
h_{FE}	DC Forward Current Gain	for ULN2801A $V_{CE} = 2\text{ V}$ $I_C = 350\text{ mA}$	1000			—	2
C_i	Input Capacitance			15	25	pF	—
t_{PLH}	Turn-on Delay Time	0.5 V_i to 0.5 V_o		0.25	1	μs	—
t_{PHL}	Turn-off Delay Time	0.5 V_i to 0.5 V_o		0.25	1	μs	—
I_R	Clamp Diode Leakage Current	$V_R = 50\text{ V}$			50	μA	6
		$T_{amb} = 70^{\circ}\text{C}$ $V_R = 50\text{ V}$			100	μA	
V_F	Clamp Diode Forward Voltage	$I_F = 350\text{ mA}$		1.7	2	V	7

TEST CIRCUITS

Figure 1a.

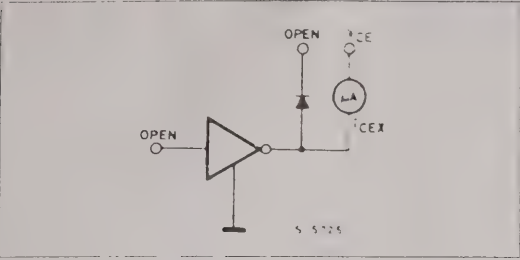


Figure 1b.

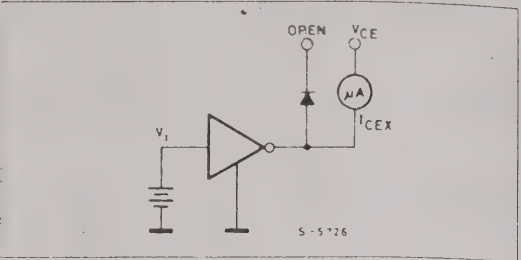


Figure 2.

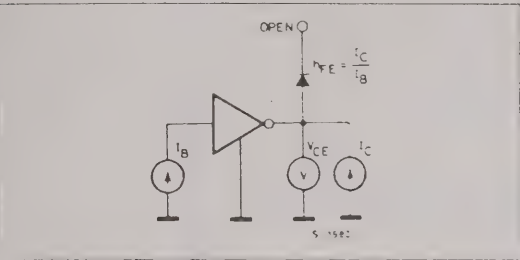


Figure 3.

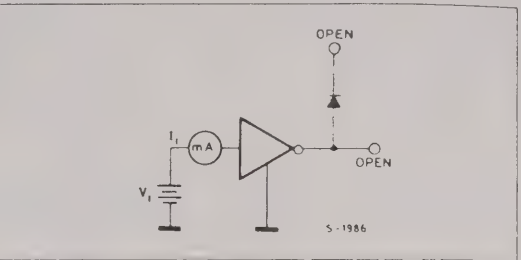


Figure 4.

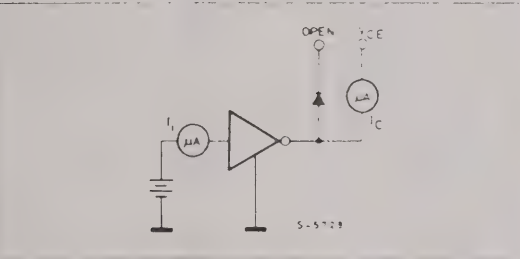


Figure 5.

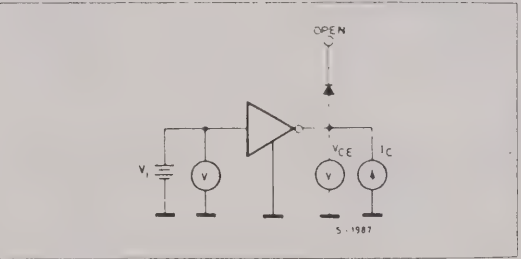


Figure 6.

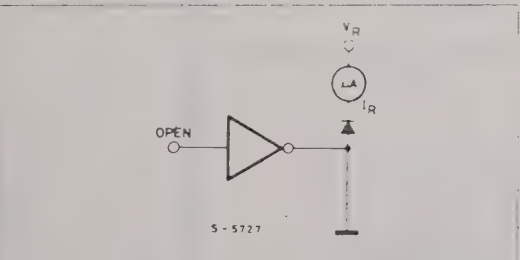


Figure 7.

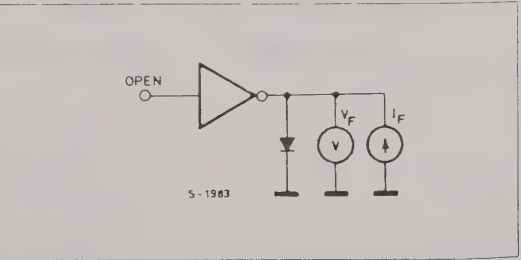


Figure 8 : Collector Current as a Function of Saturation Voltage.

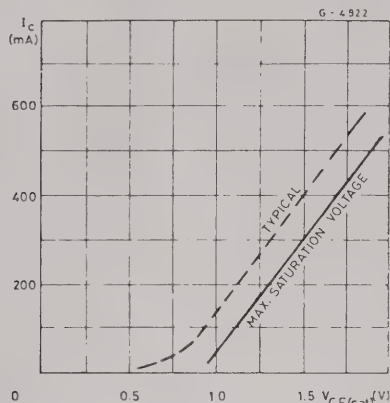


Figure 9 : Collector Current as a Function of Input Current.

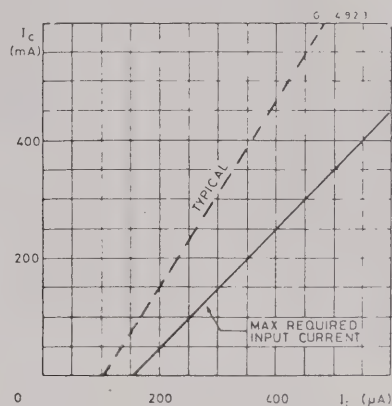


Figure 10 : Allowable Average Power Dissipation as a Function of Ambient Temperature.

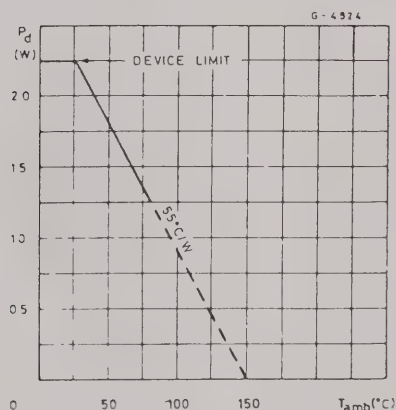


Figure 11 : Peak Collector Current as a Function of Duty Cycle.

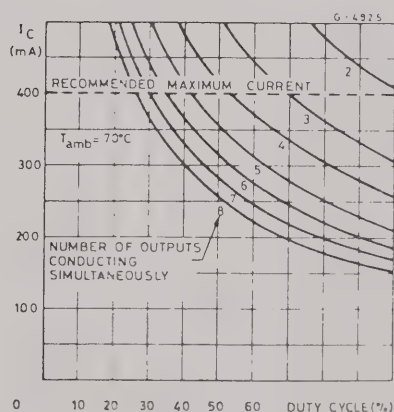


Figure 12 : Peak Collector Current as a Function of Duty.

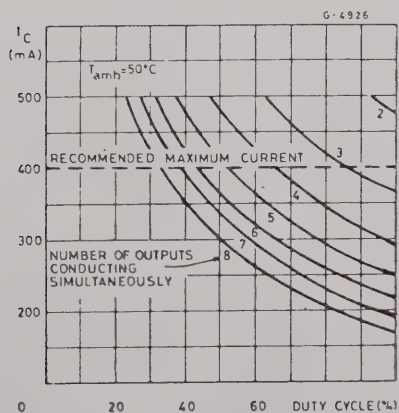


Figure 13 : Input Current as a Function of Input Voltage (for ULN2802A).

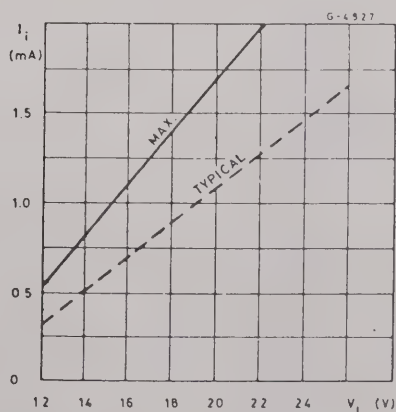


Figure 14 : Input Current as a Function of Input Voltage (for ULN2804A)

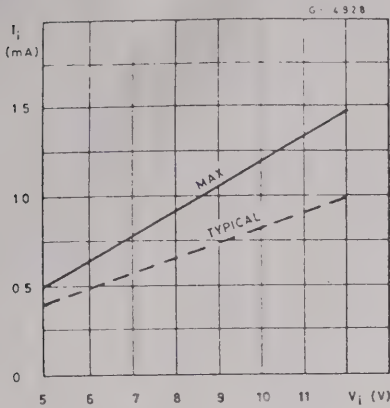


Figure 15 : Input Current as a Function of Input Voltage (for ULN2803A)

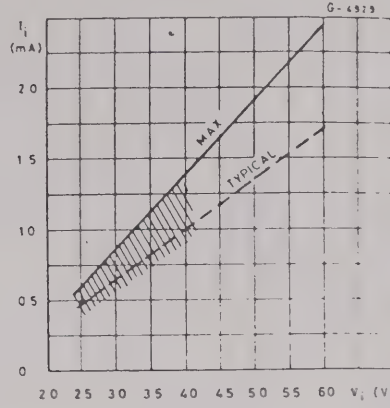
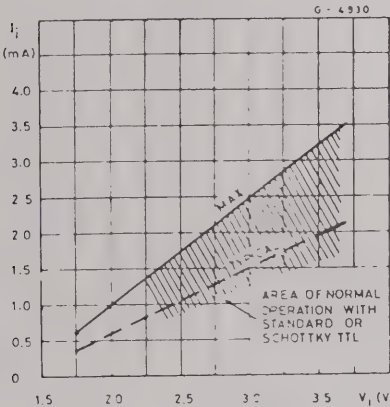


Figure 16 : Input Current as a Function of Input Voltage (for ULN2805A)



Enter text >K6EJO/R

Text is *K6EJO/R*

0086 Bits Checksum 05B8

0000 D7 71 55 44 77 C7 DD 71 75 D1 05 00 00 00 00

0010 00 00 00 00 00 00 00 00 00 00 00 00 00 00

11101011 10001110 10101010 00100010 11101110 11100011 10111011 10001110
10101110 10001011 10100000

Enter text >

\$

RUN ROM

INPUT TEXT > WA6VGZ/R & N6ECL/R

210 BITS CHECKSUM 0948

0000 D0 1D 1D 57 45 75 DC 75 DC 15 57 17 5D 00 00 00

0010 70 71 55 C4 75 D1 15 57 17 5D 00 00 00 00 00

INPUT TEXT >

>

SERIES UDN-2980A HIGH-VOLTAGE, HIGH-CURRENT SOURCE DRIVERS

FEATURES

- TTL, DTL, PMOS, or CMOS Compatible Inputs
- 500 mA Output Source Current Capability
- Transient-Protected Outputs
- Output Breakdown Voltage to 80 V

RECOMMENDED for applications requiring separate logic and load grounds, load supply voltage to +80 V, and load currents to 500 mA, Series UDN-2980A source drivers are used as interfaces between standard low-power digital logic and relays, solenoids, stepping motors, and LEDs.

Under normal operating conditions, these devices will sustain 120 mA continuously for each of the eight outputs at an ambient temperature of +50°C and a supply of +15 V. All devices in this series incorporate input current limiting resistors and output transient suppression diodes.

Type UDN-2981A and UDN-2983A drivers are for use with +5 V logic systems — TTL, Schottky TTL, DTL, and 5 V CMOS. Type UDN-2982A and UDN-2984A drivers are intended for MOS interface (PMOS and CMOS) operating from supply voltages

of 6 to 16 V. Types UDN-2981A and UDN-2982A will sustain a maximum output OFF voltage of +50 V, while Types UDN-2983A and UDN-2984A will sustain an output voltage of +80 V. In all cases, the output is switched ON by an active high input level.

Series UDN-2980A high-voltage, high-current source drivers are supplied in 18-lead dual in-line packages. On special order, hermetically-sealed versions of these devices (with reduced package power dissipation capability) can also be furnished.

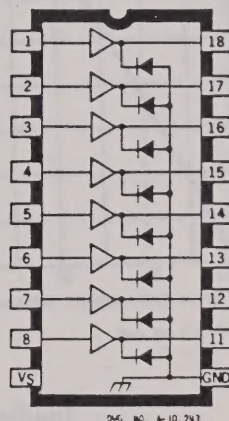


FIG. NO. 4-10-793

ABSOLUTE MAXIMUM RATINGS

Associated
LEAVITT & WELLS

